ANALYSIS AND DESIGN OF SMART PV MODULE

A Thesis

by

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ABSTRACT

This thesis explores the design of a smart photovoltaic (PV) module- a PV module in which PV cells in close proximity are electrically grouped to form a pixel and are connected to dc-dc converter blocks which reside embedded in the back pane of the module. An auto-connected flyback converter topology processing less than full power is used to provide high gain and perform maximum power point tracking (MPPT). These dc-dc converters interface with cascaded H-bridge inverter modules operating on feed forward control for dc-link voltage ripple rejection. By means of feed forward control, a significant reduction in dc link capacitance is achieved by enduring higher dc link ripple voltages. The dc link electrolytic capacitors are replaced with film capacitors thus offering an improvement in the reliability of the smart PV module. The proposed configuration is capable of producing 120V/ 240V AC voltage. The PV module now becomes a smart AC module by virtue of embedded intelligence to selectively actuate the individual dc-dc converters and control the output AC voltages directly, thus becoming a true plug and power energy system. Such a concept is ideal for curved surfaces such as building integrated PV (BIPV) system applications where gradients of insolation and temperature cause not only variations from PV module-to-PV module but from group-to-group of cells within the module itself. A detailed analysis along with simulation and experimental results confirm the feasibility of the proposed system.

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TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 Introduction

Fossil fuels dominate world energy consumption. Renewable energy is gaining popularity but is far behind in the energy race with a contribution of 2% in the global energy consumption. According to U.S. Energy Information Administration's (EIA) Annual Energy Outlook 2012, aggregate fossil fuel share of total energy consumption in U.S will fall to 77% in 2035 whereas renewable energy share will steadily increase from 8% in 2010 to 14% in 2035 [1] as can be seen from fig. 1.

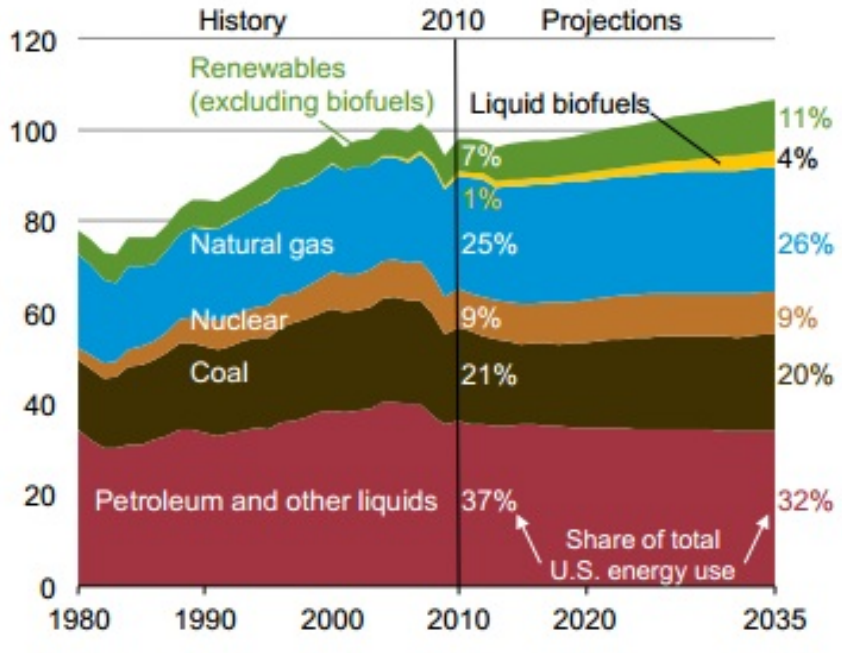


Fig. 1 Primary energy use by fuel, 1980-2035 (quadrillion Btu) taken from [1]

The paradigm shift in focus from the conventional fuel to the unconventional sources has prompted from the need to reduce carbon emissions, prevent further

depletion of fossil fuel reserves and address visible indirect effects like global warming, ozone layer depletion, climate change etc.

Renewable energy is abundant, sustainable, clean and can be harnessed from different sources in the form of wind, solar, tidal, hydro and biomass. However, key issues like intermittency in supply, resource location and cost of renewable on a dollar-per-kilowatt-hour basis are the main roadblocks preventing it from entering the mainstream energy. At this level, produces and consumers, policy makers and governments have an important role to play in addressing the challenges associated with the development of renewable energy.

Solar photovoltaic (PV) is an integral part of the renewable energy sector and has witnessed tremendous growth in the past decades as evident from fig. 2.

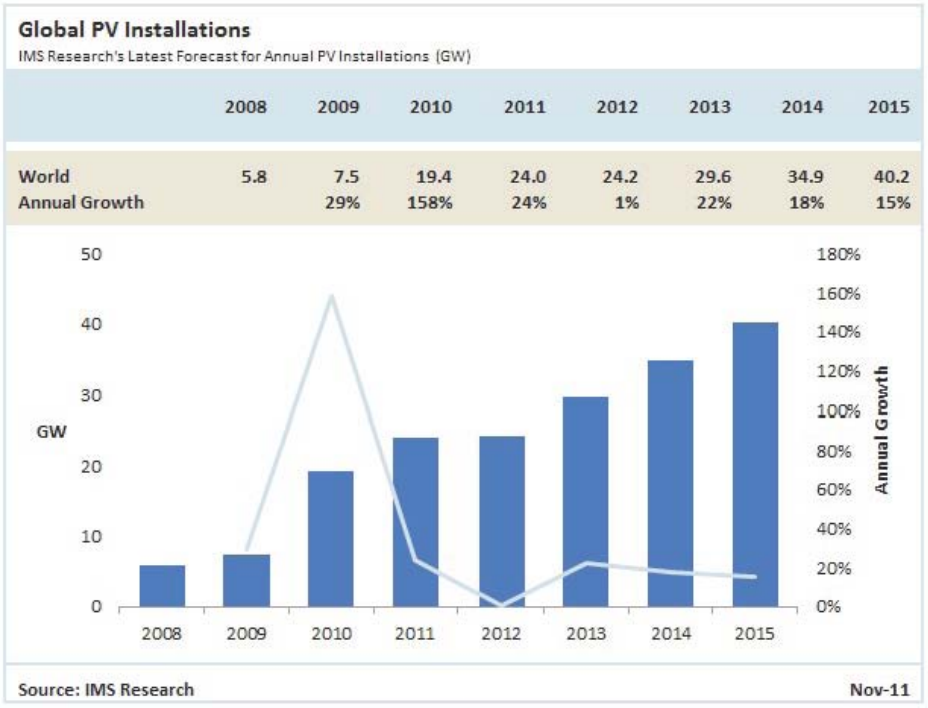


Fig. 2 Global PV installations taken from [2]

From fig. 2 it can be seen that the PV installations from 2008 to 2012 have grown more than four times and will touch 40.2GW in 2015. Therefore, to address the rapid growth in PV installations, there is a lot of scope of improvement in the area of power conditioning of the solar photovoltaic. Important factors affecting the power conditioning of photovoltaic systems are the growing energy demand, deployment at various levels- residential, commercial and utility scales, efficiency, reliability, flexibility and control, policies and cost competitiveness to name a few.

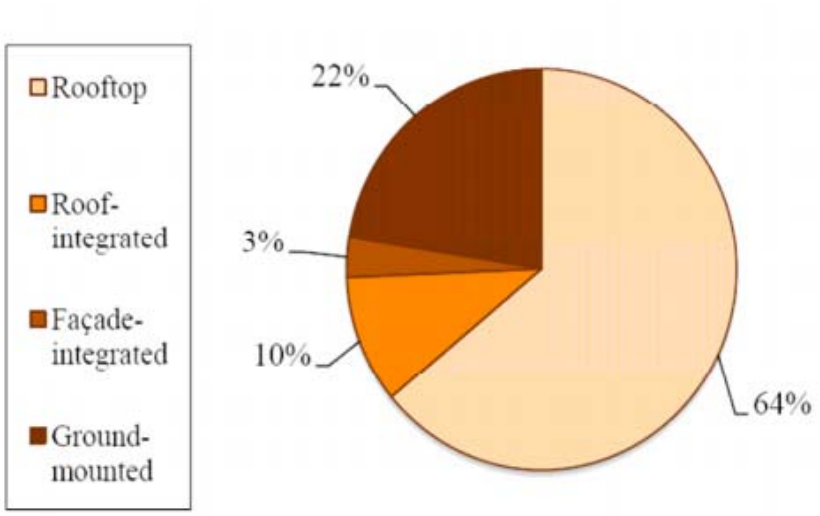


Fig. 3 US PV installations - 2008 Market Shares taken from [3]

Fig. 3 shows 2008 market shares for PV installations in US. It can be seen that roof top installations which mainly manifest in the form of residential systems dominate the US PV market where as ground-mounted installations in the form of utility scale PV have a very low market share. Therefore, it is important to focus on the power conditioning of residential PV systems and evaluate the current state of the art power conditioning technologies and understand the scope of their improvement.

1.2 Solar resource

The sun is a gigantic, 1.4 million kilometer diameter, thermonuclear furnace fusing hydrogen atoms into helium and the loss of mass due to fusion is converted into about 3.8 × 1020 MW of electromagnetic energy that radiates into space [4].

Photovoltaic material is capable of converting the energy contained in photons of light into electricity. A photon with short wavelength and high energy can cause an electron in a photovoltaic material to break free of the atom that holds it and if a nearby electric field is provided, those free electrons can be swept toward a metallic contact where they can emerge as an electric current [4].

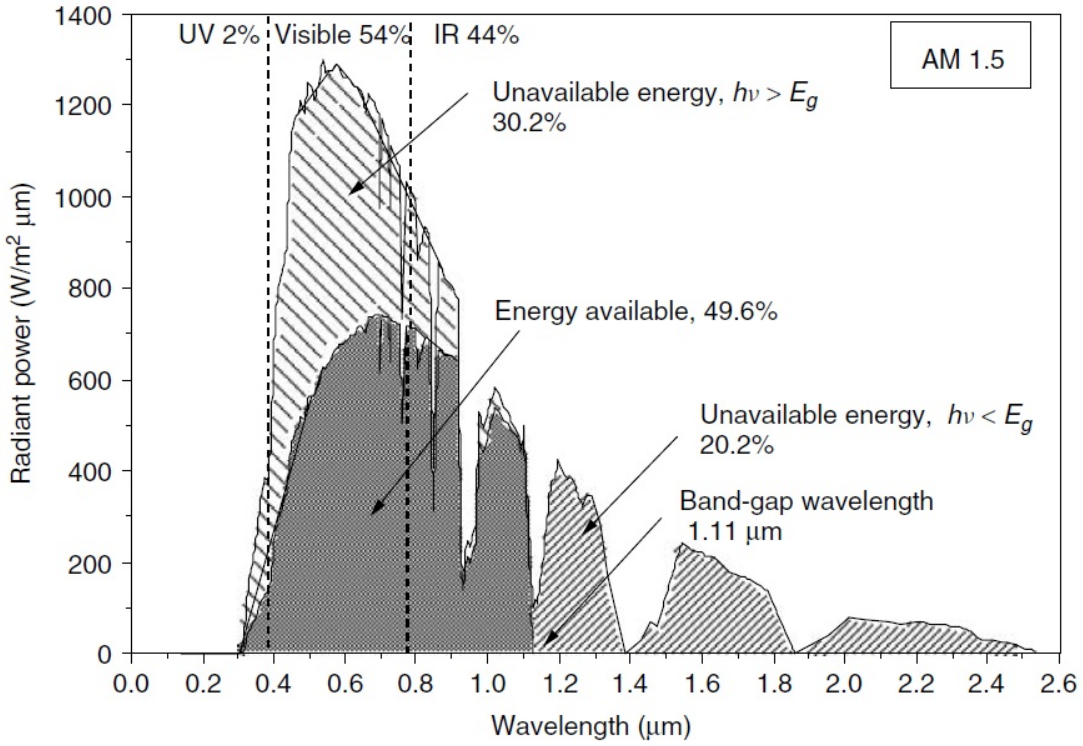


Fig. 4 Solar spectrum at AM 1.5 taken from [4]

An air mass (AM) ratio of 1 indicates that the sun is directly overhead. For most photovoltaic work, an air mass ratio of 1.5, corresponding to the sun being 42 degrees above the horizon, is assumed to be standard [4]. Fig. 4 shows the solar spectrum at 1.5AM. For an AM 1.5 spectrum, 2% of the incoming solar energy is in the UV portion of the spectrum, 54% is in the visible, and 44% is in the infrared [4].

1.3 Model of solar cell

A simple equivalent circuit model for a photovoltaic cell consists of a real diode in parallel with an ideal current source as shown in Fig. 5. The ideal current source delivers current in proportion to the solar flux to which it is exposed.

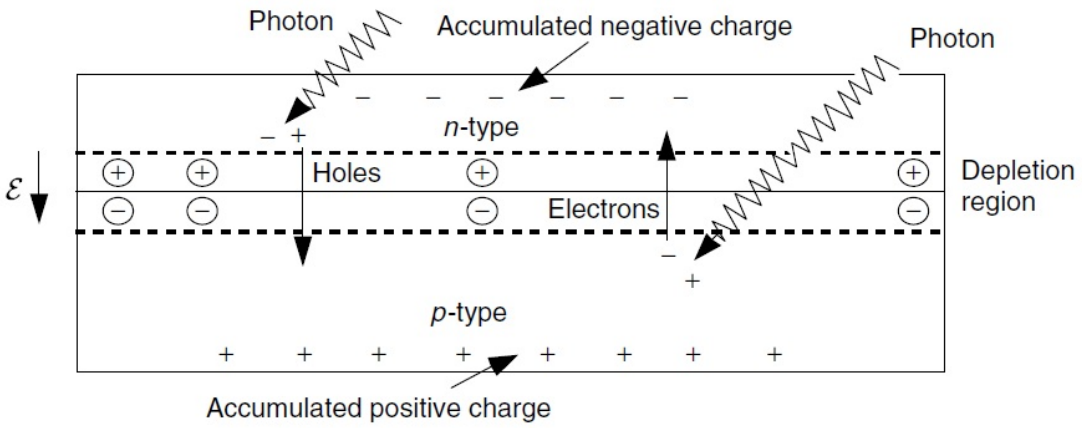


Fig. 5 Model of a photovoltaic cell taken from [4]

A more accurate equivalent circuit of the photovoltaic cell consists of a parallel leakage resistance, R_p and a small series resistance, R_s and is shown in fig.6.

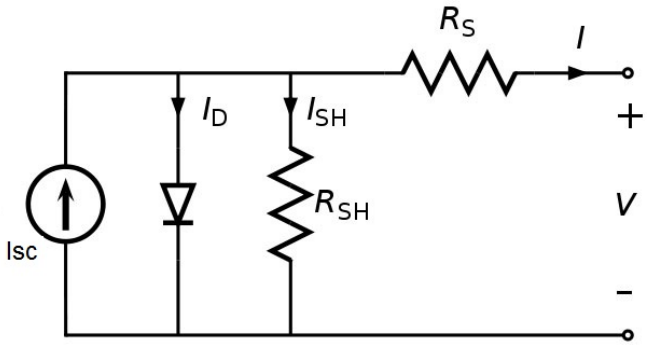


Fig. 6 Equivalent circuit of PV cell

The output current of the PV cell can be represented as:

$$I = I_{sc} - I_o \left\{ exp\left[\frac{q(V+IR_s)}{kT}\right] - 1 \right\} - \left(\frac{V+IR_s}{R_p}\right) \quad (1)$$

Where I_{sc}: short circuit current, I_o: diode reverse saturation current, q: electronic charge (1.602 x 10^-19C), k: Boltzmann's constant (1.381 x 10^-23J/K), T: junction temperature (K), V: Output voltage, R_s : series resistance, R_p: parallel resistance

1.4 Research objective

The objective of this thesis is to develop the new technology of smart PV module for the power conditioning of solar photovoltaic for residential applications. The concept of smart PV module involves grouping a small number of PV cells within the module called pixels and power conditioning them with dedicated dc-dc converters. The dc-dc converters now process much lower power than the overall rated power of the entire module. Hence, the power electronics for this application can capture the low power IC industry. Moreover, since the entire power electronics is embedded within the module itself, smart PV module offers the advantage of an easy plug and power system. This

takes the power conditioning technology a step further than the present day micro-inverter technology.

The power architecture of the smart PV module consists of auto-connected flyback based dc-dc converters connected to each pixel and series connected inverters to produce split phase 120V/ 240V grid tied mains voltage. The auto-connected flyback converters are responsible for performing localized maximum power point tracking and boosting the input pixel voltage. The series connected inverters form a multi-level cascaded inverter feeding in the voltage boosted by the flyback converters. A feed forward control approach is proposed to dynamically compute the modulation index of the inverter based on the sensed DC link voltage. This allows the capacitance of the DC link capacitors to reduce considerably as they are now made to withstand higher ripple voltage on the DC link voltage bus. The overall system reliability is also improved by replacing the electrolytic dc link capacitors with film capacitors due to reduced size of dc link capacitors. The simulation and the experimental results will be obtained to prove the feasibility of the proposed system. A subsection of the proposed system will be built as the laboratory prototype and will be tested using solar cells. The control will be implemented by using TMS320F28035 digital signal processor (DSP) to validate the control schemes.

1.5 Thesis outline

Section 1 of the thesis presents an overview of the energy consumption scenario of the world and the position taken by renewable energy. It has also been identified that

residential applications in the form of roof mounted and roof integrated photovoltaic are the most prevalent form of PV installations in US. It also briefly describes the solar resource and how it can be harnessed in the form of the photovoltaic cell. Finally, the research objectives of this work are presented.

Section 2 presents in depth description of the evolution of the different power conditioning topologies till date and a comparison is drawn for the different topologies based on a number of important factors for residential applications.

Section 3 introduces the work of this thesis, the concept of smart PV module. It discusses the advantages of the smart PV module and its possible power configurations. The latter part of the chapter is dedicated towards discussing the overall power architecture of the smart PV module consisting of dc-dc converter topology and the inverter topology.

Section 4 discusses the overall control scheme of the smart PV module with individual focus on the maximum power point tracking algorithm employed, the control of the dc-dc converters and feed forward control of the inverters for DC link voltage ripple rejection. Subsequently, the chapter discusses the effect of the inverter control strategy on the amount of dc link voltage ripple tolerated, size reduction of the DC link capacitors and the aspect of system reliability.

Section 5 presents a design example for a residential scale solar PV module followed by the simulation results of the overall system. A major part of the chapter discusses the hardware implementation of the smart PV module. Experimental results of the laboratory prototype are also discussed.

Section 6 provides the general conclusion of the work and discusses the scope and future work.

2. REVIEW OF PHOTOVOLTAIC CONVERTER TOPOLOGIES

2.1 Introduction

Power conditioning for solar photovoltaic modules has undergone a tremendous development in the recent years to keep pace with emerging technologies and the growing PV industry [5], [6]. This section discusses the past and present day PV converter topologies and also technologies that can be adopted in the future.

2.2 Centralized converter topology

Past technology was based on centralized PV converters that interfaced a large number of PV modules to the grid [5]. The PV modules were connected in series to form strings, each generating a sufficiently high voltage. These strings of PV modules were then connected in parallel, through string diodes, in order to reach high power levels shown in fig. 7. This centralized inverter includes some disadvantages, such as high-voltage dc cables between the PV modules and the inverter, low energy harvest due to a centralized MPPT, mismatch losses between the PV modules, losses in the string diodes, and a nonflexible design where the benefits of mass production could not be reached [5]. The grid-connected stage was usually line commutated by means of thyristors, involving many current harmonics and poor power quality [5].

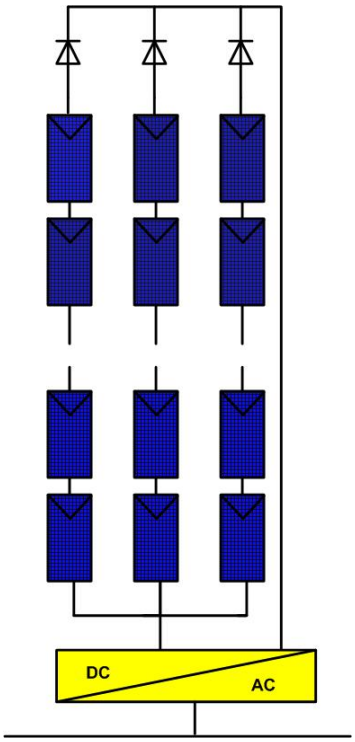


Fig. 7 Centralized converter topology

2.3 String and multi string converter topologies

The present technology consists of the string inverters and the ac module [5]. The string inverter, shown in Fig. 8(a), is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter. The normal operation voltage is approximately 450 - 510 V. The possibility of connecting fewer PV modules in series also exists, if a dc–dc converter or line-frequency transformer is used for voltage amplification required for the inverter operation. There are no losses associated with string diodes as they are eliminated by the use of converters and separate MPPTs can be applied to each string. This increases the overall efficiency compared to the centralized inverter and reduces the price, due to mass production.

The multi-string inverter depicted in Fig. 8(b) is the further development of the string inverter, where several strings are interfaced with their own dc–dc converter and then to a common dc–ac inverter, [5]. This is advantageous as compared to the centralized system, since every string can now be controlled individually. Thus, the operator may start the PV power plant with a few modules. Further enlargements are easily achieved since a new string with dc–dc converter can be plugged into the existing platform offering high flexibility. However, both string and multi-string topologies add complexity of the system and overall efficiency reduces due to more number of power processing stages [5].

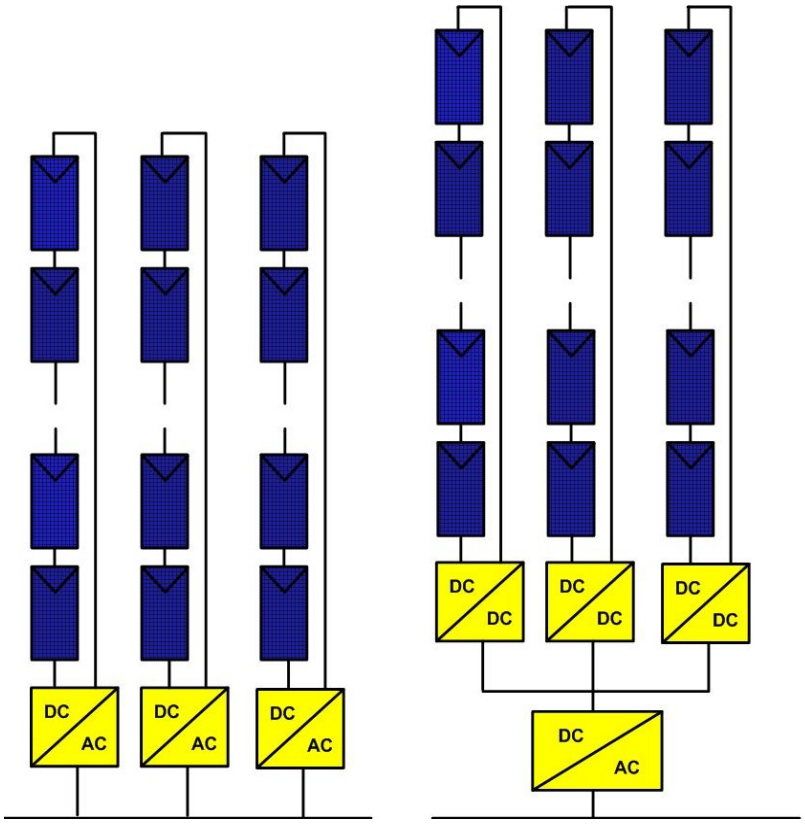


Fig.8(a) String converter topology (b) Multi-string converter topology

2.4 Microinverter technology

The present micro-inverter technology is the integration of the inverter and PV module into one electrical device and is shown in fig. 9. It removes the mismatch losses between PV modules since there is only one PV module for every converter, as well as supports optimal adjustment between the PV module and the inverter and, hence, the individual MPPT. It includes the possibility of an easy enlargement of the system, due to its modular structure. It has the potential to become a "plug-and-power" device, which can be used by persons without any knowledge of electrical installations, is also an inherent feature [5], [7]-[10].

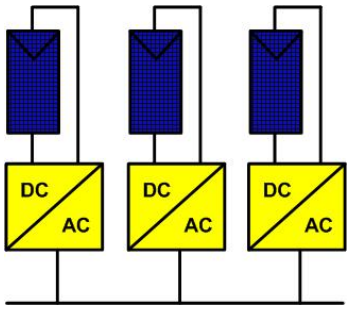


Fig. 9 Microinverter technology

On the other hand, microinverter calls for high voltage-amplification which may reduce the overall efficiency and increase the price per watt, because of more complex circuit topologies. On the other hand, the ac module is intended to be mass produced, which leads to low manufacturing cost and low retail prices [5].

2.5 AC solar cell technology

The ac cell is the case where a complete PV system is constructed from lateral multi-junction solar cells using a new interconnection technique shown in fig.10 [11]-[12]. The main challenge in this technology is to develop an inverter that can amplify the very low voltage up to an appropriate level for the grid, and at the same time reach a high efficiency. Moreover, such a concept involves sophisticated fabrication process at the solar cell level and complex circuitry embedded in the silicon.

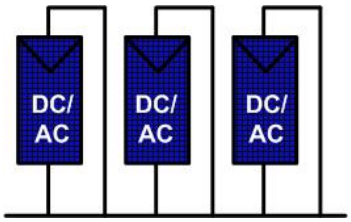


Fig. 10 AC solar cell technology

2.6 Comparison of technologies

The photovoltaic power conditioning topologies described in the previous subsections have different operating regimes. Hence, they differ based on factors like power range, reliability, efficiency, scalability and cost to name a few [13] based on the application targeted. Table 1 shown below provides an overview of the comparison between different technologies based on a number of factors important for the evaluation of the different technologies for residential applications.

Table 1 Comparison of different power conditioning technologies

Factor		Centralized Topology	String Topology	Multi-String Topology	Microinverter Technology	AC Solar Cell
Power Range		*High* Small scale & utility scale	*Medium* Small scale & utility scale	*Medium* Small scale & utility scale	*Low* Small Scale	*Low* Small scale
System Scalability		*Very Low* Non-flexible design	*Medium* Flexible design based on string size	*Medium* Flexible design based on string size	*High* Modular and allows plug & play option	*Very Low* No flexibility for scaling as design is at the silicon level of the cell
System Efficiency		*Medium* High power range, accounts for mismatch losses, losses due to string diodes etc.	*Very High* High power range, no losses due to string diodes	*Medium* Reduced efficiency due to two stage power processing	*High* Reduced efficiency due to low power range, high voltage amplification, but no mismatch, string diode based losses	*High* Reduced efficiency due to lower power range, high voltage amplification, but no mismatch, string diode based losses
MPPT Effectiveness		*Low* Losses due overall centralized MPPT	*Medium* Less losses due string level MPPT	*Medium* Less losses due string level MPPT	*High* Improved module level MPPT	*Very High* Highly improved localized cell level MPPT
Reliability	**No. of components**	*Very High* Involves just one centralized converter	*High* Involves one converter stage/ string	*Medium* Involves two converter stages / string	*Low* Involves a converter stage/ module	*Very Low* Involves a converter stage/ cell
	Single module failure	*Very Low* Failure of centralized converter affects the whole system	*Medium* Failure of string converter affects one string	*Low* Failure of multi-string converter affects a number of strings	*High* Failure of micro-inverter affects only one module	*Very High* Failure of one PV cell inverter affects only one cell
Hardware Requirement		*Very Low* Involves one bulky converter, dc cables between modules	*Low* Involves hardware for every string for the entire system	*Medium* Involves more hardware/ string than String topology	*High* Involves hardware/ module for the entire system	*Very Low* Does not require any hardware as the power processing is at the Silicon

Table 1 Continued

					level
Manufactura-bility	*Low* Bulky system, mass production is difficult	*Medium* Mass production is possible	*Medium* Mass production is possible	*High* Modular, mass production is possible	*Low* Mass production is possible but very sophisticated manufactur-ing process
BOM Cost	*Low* Involves least number of stages and simple control	*Medium* Involves more hardware and individual control	*Medium* Involves more hardware and individual control	*High* Involves hardware/ Module and individual control	*Very High* Technology is in nascent stage, high production cost

From table 1, it is clear that microinverter technology flairs well for a number of aspects such as MPPT effectiveness, system scalability, manufacturability and overall system efficiency for residential PV application.

2.7 Conclusion

The features of the prevalent power condition topologies in today's market have been described. A comparison of the different topologies has been drawn based on important factors such as power range, system size, MPPT effectiveness, reliability for residential PV applications.

3. ANALYSIS OF PROPOSED SMART PV MODULE

3.1 Introduction

In smart PV module, groups of cells within a PV module are power conditioned by dedicated low power integrated dc-dc converters. Fig.11 illustrates the front and back view of the smart PV panel. It is seen that in the front pane of the panel a group of cells

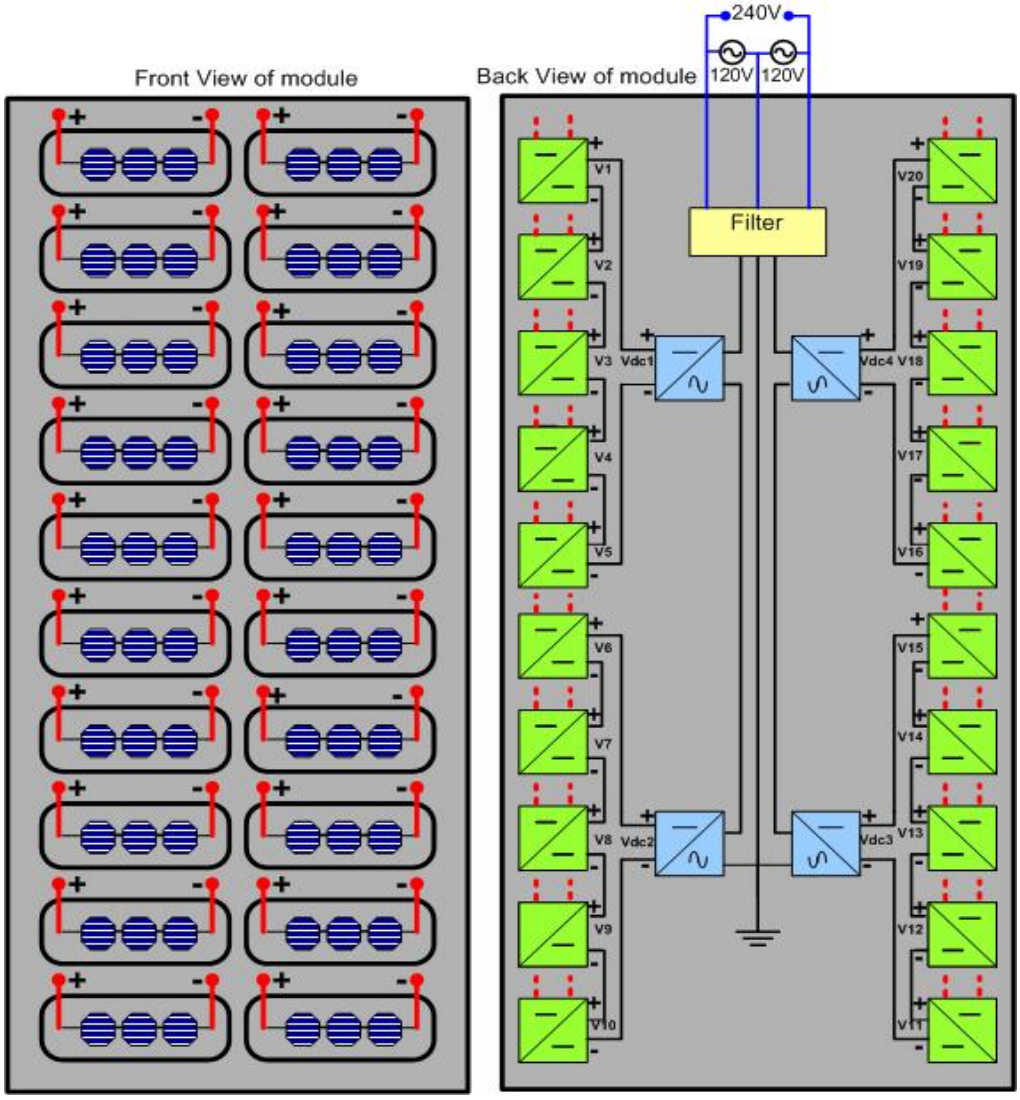


Fig.11 Front and back view of smart PV module

are electrically interconnected to form a *pixel*. Each pixel has two electrical terminals which connect to dc-dc converters embedded in the back pane of the panel shown in dotted lines. The output of these converters are series connected and fed into H-bridge inverter modules to produce 120V/240V AC grid tied mains voltage.

The advantages of the proposed smart PV panel are:

- The power electronic circuitry along with MPPT algorithm associated with each pixel can be combined within a monolithic IC.
- The approach enables easy integration of PV modules of any type in series/parallel configurations to suite an end user application.
- It has the potential to incorporate intelligence to communicate important date to the user and manage information interchange between the panels.
- The entire system operates optimally when installed on curved surfaces such as in BIPV systems employing thin film PV arrays.
- Since MPPT is now optimized at a sub-module level, the overall energy harvesting efficacy is greater. Partial shading within each module can be easily dealt with. There is no longer any need for matching and individual module degradations are handled locally.
- Modules can be optimized independently of the system – the auto-connected flyback converters can be configured to provide the desired system voltage leaving the selection of the exact number of cells unconstrained to allow for various physical sizes of modules and cell technologies.

3.2 Possible power configurations

In the proposed concept, an optimized number of cells in close proximity are electrically grouped to form a pixel and embedded low power dc-dc converters are co-located within the PV module. Power configuration of the smart PV module consists of determining the size of a pixel and the number of pixels with their dedicated converters required in a module. A number of power architectures are possible for a given module by varying the pixel size. It is possible to bifurcate the module into 'n' pixels and have 'n' converters associated with the module.

This concept is illustrated by considering the following example using Sharp's NU-Q235F2 PV module. The module has 60 cells in series, maximum power of 235W at 25ºC, maximum power voltage of 30V and maximum power current of 7.84A. Table 2 provides data obtained from simulation for the possible power configurations at 1 sun.

Table 2 Possible power configurations for Sharp's NU-Q235F2 PV module

No. of pixels	**No. of cells/pixel**	**No. of converters/module**	**Vmpp / pixel (V)**	**Pmpp/ pixel (W)**
60	1	60	0.515	3.92
30	2	30	1.08	7.84
20	3	20	1.51	11.75
15	4	6	2.09	15.7
12	5	12	2.58	19.58
10	6	10	3.07	23.5
6	10	6	5.08	39.2
5	12	5	6.06	47
4	15	4	7.55	58.75
3	20	3	10.1	78.33
2	30	2	15.02	117.5

It can be seen that the power handled by each converter varies with respect to the pixel size and hence affects the power rating of the converter used. The power rating for

the converters is restricted to a maximum of 20W as the concept of smart PV panel targets the low power IC industry exclusively.

3.3 Proposed dc-dc converter topology

The dc-dc converter topology chosen for this application has to meet conflicting requirements: high voltage gain and high overall efficiency over a wide range of solar insolation. Further, module integrated power electronics have to withstand higher temperatures while exhibiting fault tolerant and a failsafe failure mode to maintain system availability. A suitable topology for the power converter is the auto-connected flyback converter. Flyback converter, shown in fig. 12 is a transformer isolated version of the buck-boost converter which can be used to give very high voltage gain [13]-[15].

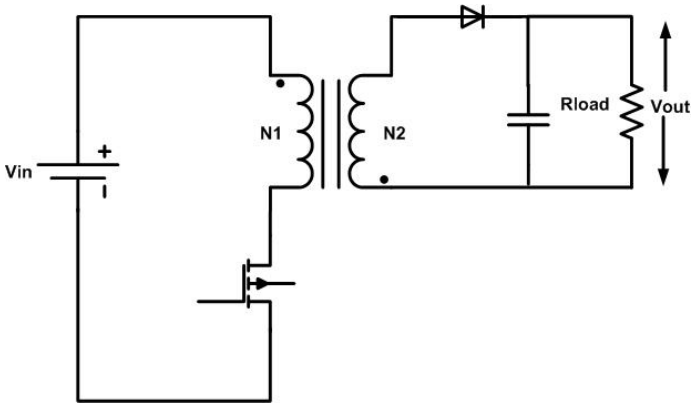


Fig. 12 Flyback converter

Auto-connected flyback converter, shown in fig. 13 is derived from the flyback converter by taking the output across the positive of the input voltage and the secondary capacitor voltage. In this way, the overall output voltage also includes the input voltage

thus providing higher gain. The same auto-connected flyback converter can be redrawn as shown in fig. 14.

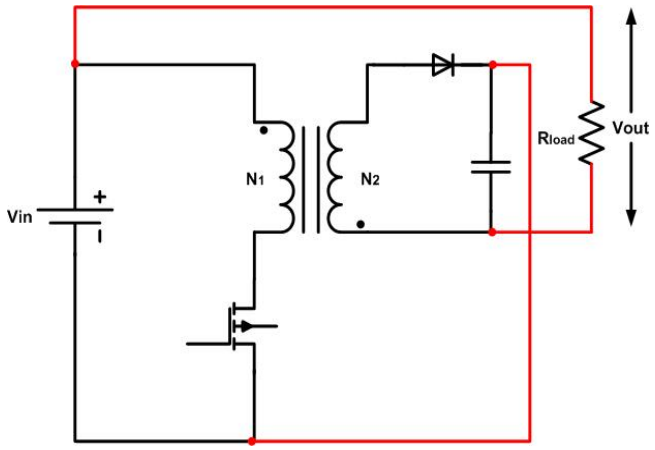


Fig. 13 Auto-connected flyback converter derived from flyback converter

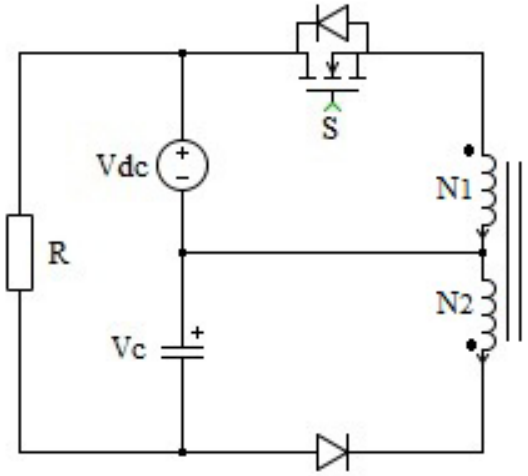


Fig. 14 Auto-connected flyback converter

Further, the efficiency of the auto-connected flyback converter is increased as a part of the input power is directly fed forward to the output, thus the converter processes less than full-power but foregoes isolation [16]-[18].

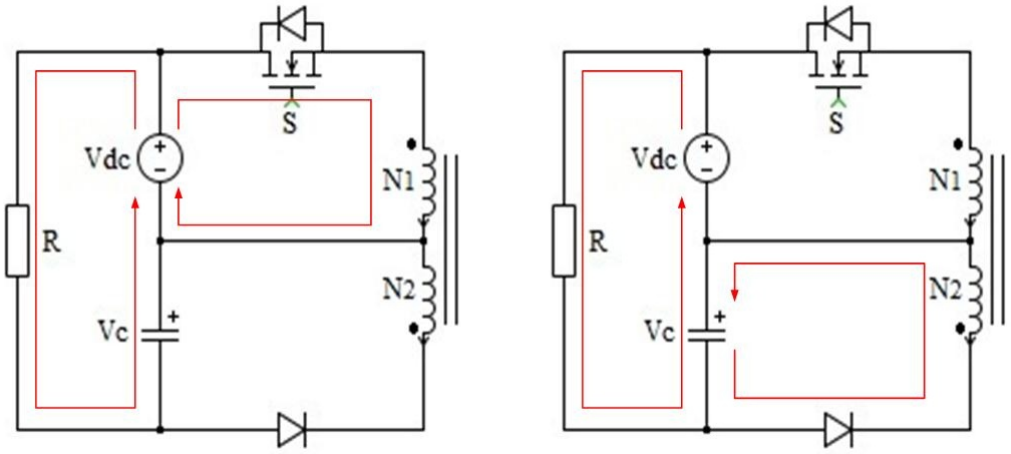


Fig. 15 Operation modes of auto-connected flyback converter

Fig. 15 shows the modes of operation of the auto-connected flyback converter. For boost operation, transformer secondary turns n_2 is chosen to be greater than primary turns, n_1.The voltage gain of the converter is given by:

$$\frac{V_o}{V_{in}} = \frac{D}{D'}\frac{n_2}{n_1} + 1 \qquad (2)$$

At low power, switching frequencies in MHz range are easily possible, which allows the transformer size to be considerably reduced. Silicon carbide (SiC) based MOSFETs and diodes can be used for this application for withstanding high temperature conditions.

3.4 Inverter topology

The simple H-bridge inverter topology is used for the second stage power conversion [19]. The inverters are connected in series to form four stage cascaded inverter topology and is shown in fig. 16. The output line voltage, V_{rms} produced by

each inverter module depends on the DC link voltage input voltage, Vdc and the modulation index, M_a chosen and is given by:

$$V_{rms} = \frac{M_a Vdc}{\sqrt{2}} \tag{3}$$

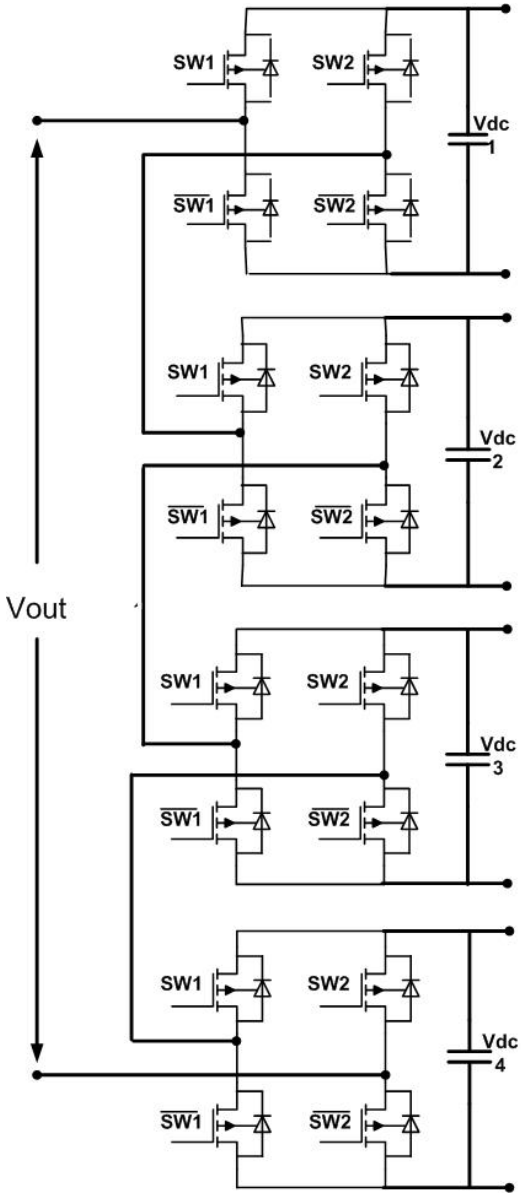


Fig. 16 4 stage cascaded H- bridge inverter

Each inverter is modulated with phase shifted carriers to obtain multi level output voltage shown in fig. 17. The inverter operates using unipolar modulation scheme which results in significantly lower harmonic content [20]. Unipolar modulation involves the following control voltages which are compared with the carrier signal, V_{tri} to obtain the switching signal to be given to the gates of the four mosfets involved in one H-bridge inverter.

$SW_1: V_{control} > V_{tri}$

$SW_2: -V_{control} > V_{tri}$

$\overline{SW_1}: V_{control} < V_{tri}$

$\overline{SW_2}: -V_{control} < V_{tri}$

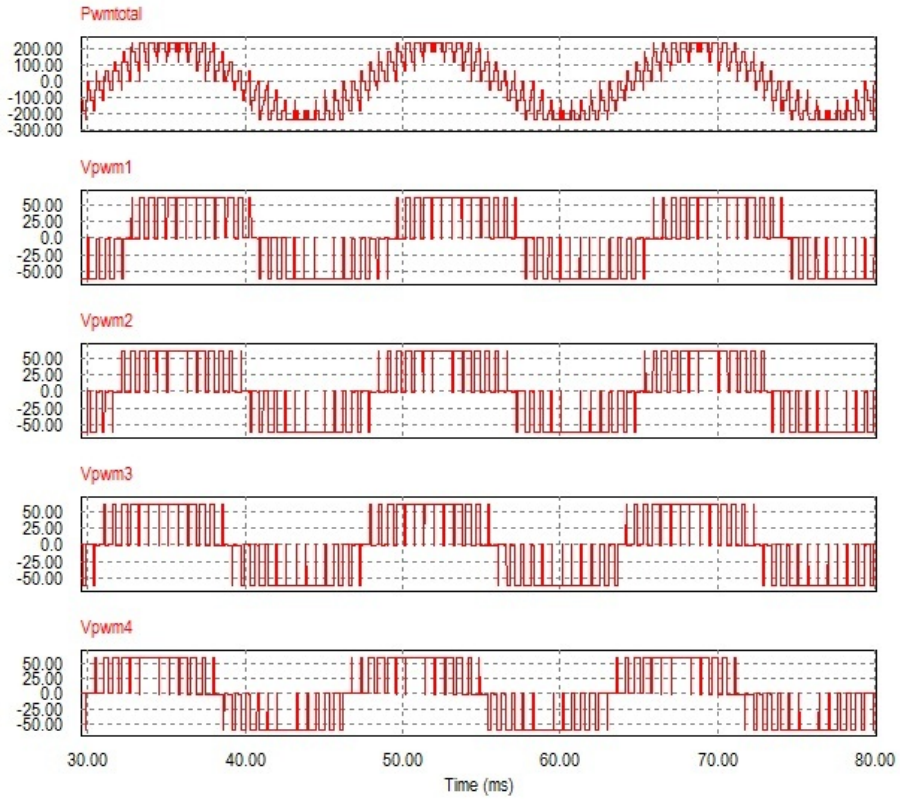


Fig. 17 Output phase PWM voltages of 4 stage cascaded H-bridge inverter

Multilevel inverters have the advantages of low output distortion and EMI. Voltage stress on the inverter switches of each stage is a fraction of the overall voltage rating, allowing high performance devices with low voltage rating and improving efficiency [20].

3.5 Overall system architecture

The power architecture of smart PV module consists of the dc-dc converters and the inverter modules along with their associated control circuitry. Fig. 18 shows the power architecture of the overall system for the three cell/pixel configuration discussed in section 3.2. The PV pixel serves as the input to each auto-connected flyback converter. Each H-bridge inverter interfaces with five auto-connected flyback converters connected in series. These inverters are then connected in series to form a four stage cascaded inverter capable of producing 240V AC voltage. The inverter is centrally grounded to provide split phase 120V AC voltage output.

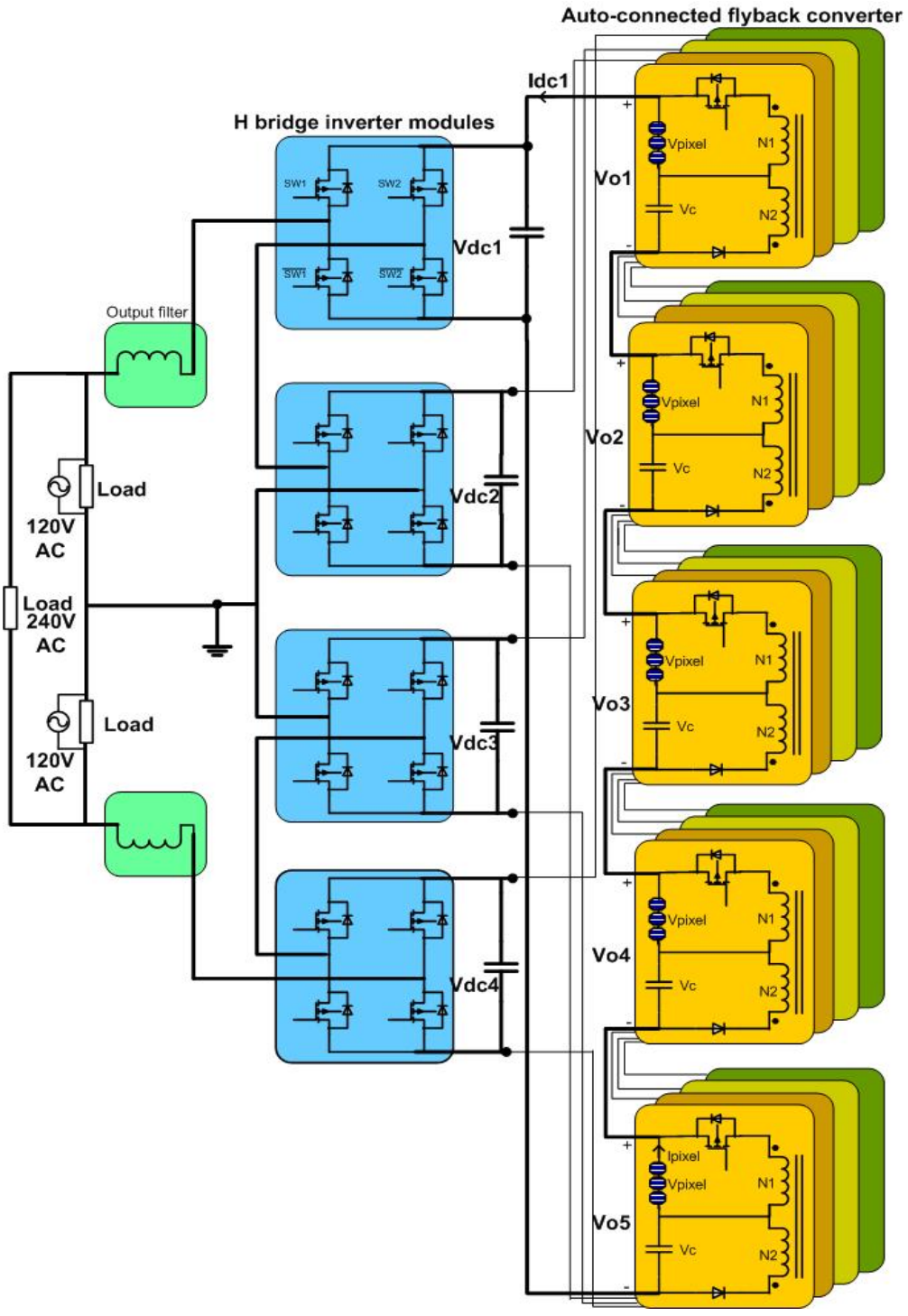


Fig. 18 Overall system architecture of smart PV module

3.6 Conclusion

The proposed concept of smart PV module has been explained along with its features. The possible power configurations of the smart PV module have been explored. An auto-connected flyback converter topology has been chosen for the DC stage to meet the requirements of high voltage gain at varied insolation, low component count and high efficiency. A cascaded H bridge inverter topology with phase shifted carriers is selected for the AC stage. The overall system architecture has been described for three cell/ pixel configuration.

4. CONTROL OF SMART PV MODULE

4.1 Introduction

The overall control scheme for the smart PV module is designed to provide simple flexible control, reduce hardware and sensing requirements and improve reliability of the system. The block diagram of the overall control scheme is illustrated in fig. 19. The functional overview of each controller is listed below.

1. Implementation of MPPT algorithm at the DC stage for transferring maximum power at any particular insolation.
2. Control of auto-connected flyback converter for boosting the input pixel voltage and optimally operating at the MPPT point.
3. Feed forward control of inverter modules for producing split phase 120V/240V AC voltage.

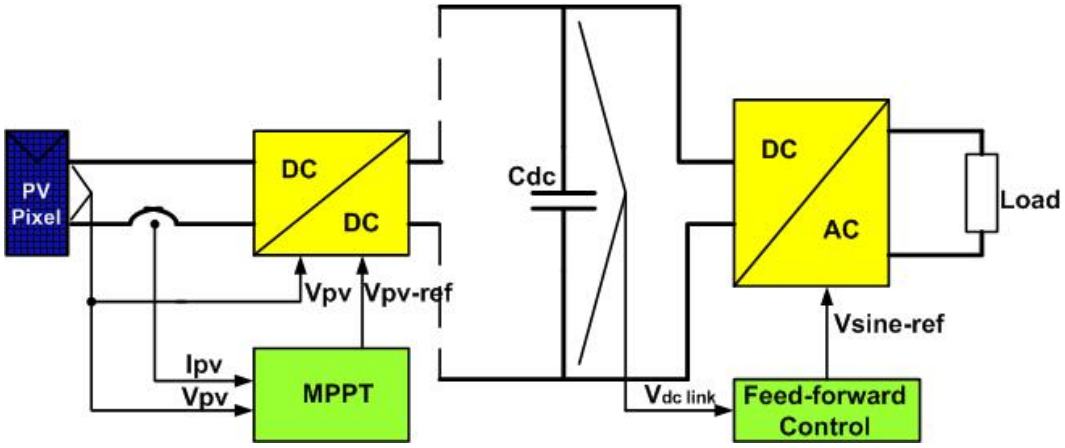


Fig. 19 Overall control block diagram of smart PV module

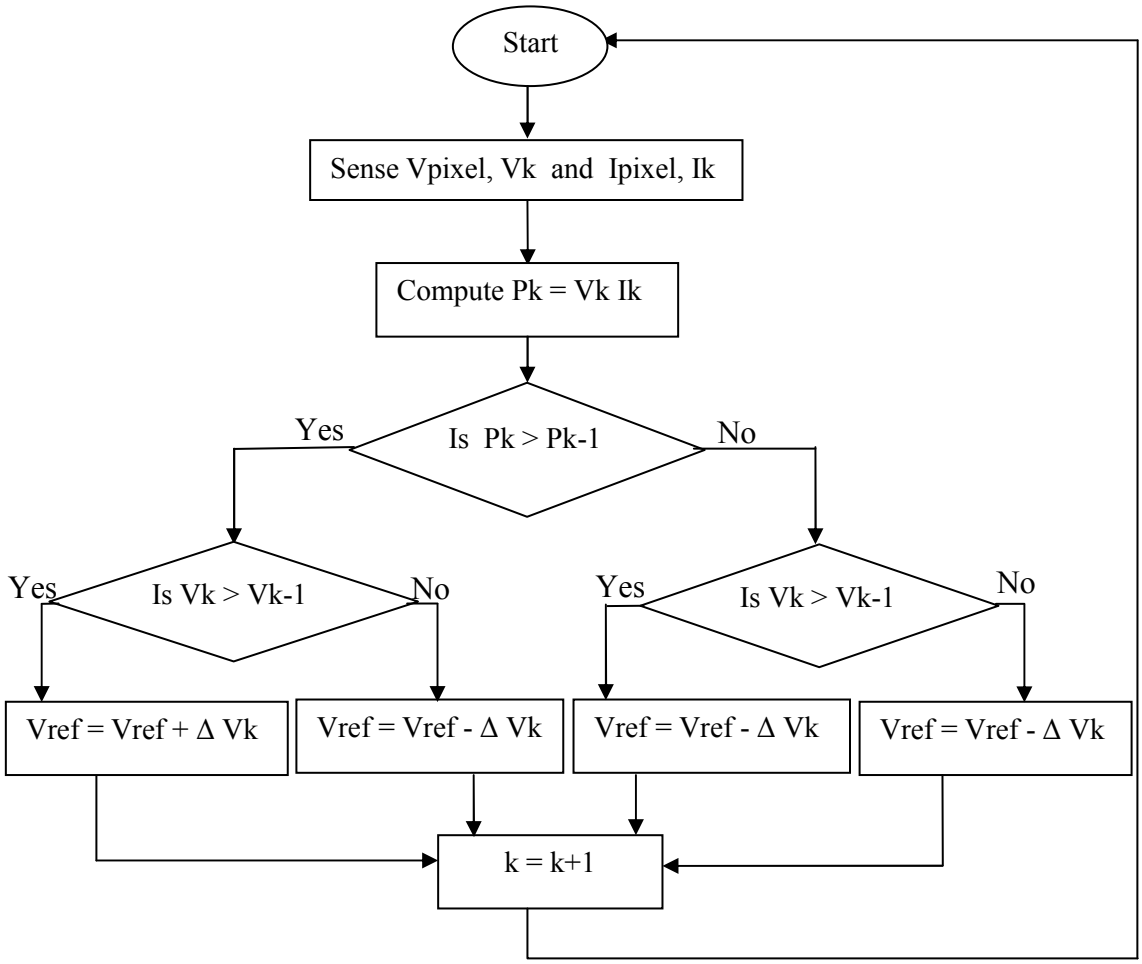
4.2 MPPT algorithm

Under varying solar insolation and shading conditions, the V-I characteristics of the PV cells vary widely. The flyback converter interface to a small group of PV cells in smart PV module needs to be suitably controlled to produce a high output voltage while maintaining a high operating efficiency. Embedded along with the switch-level control of the flyback converter is the MPPT algorithm. Numerous techniques have been proposed [21] with different tracking efficacies and implementation requirements. Since most of the techniques offer good performance, the key selection criterion is ease of implementation since it is desirable to avoid having to add extra components or sensors to the converters.

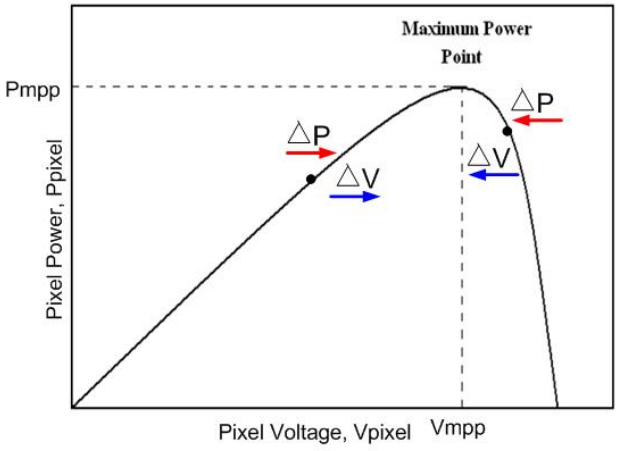
Perturb and Observe (P&O) MPPT algorithm is chosen due to its low implementation complexity. In P&O, a perturbation is introduced in the PV pixel operating voltage. A change in the pixel voltage, affects a change in the PV current based on the V-I curve of the PV module and hence the power. The P-V curve of the PV module is shown in fig. 20. The algorithm continuously seeks the maximum power point at each perturbation by evaluating the current power and comparing with the power at the previous operating point [22]-[23]. Table 3 shows the voltage perturbation and how the algorithm decides the next perturbation for MPPT.

Table 3 P&O MPPT algorithm implementation

Current Perturbation	**Change in Power**	**Next perturbation**
+ ΔV	+ ΔP	+ ΔV
+ ΔV	-ΔP	- ΔV
- ΔV	+ ΔP	- ΔV
- ΔV	-ΔP	+ ΔV



(a)



(b)

Fig. 20 (a) P&O MPPT algorithm (b) P-V curve of a photovoltaic module

The effectiveness of the MPPT algorithm is tested by simulating one flyback converter with a pixel voltage as its input and implementing a step change in insolation from 0.1 sun to 1 sun. Fig. 21 shows the V-I and P-V curves of the PV pixel under the change in insolation.

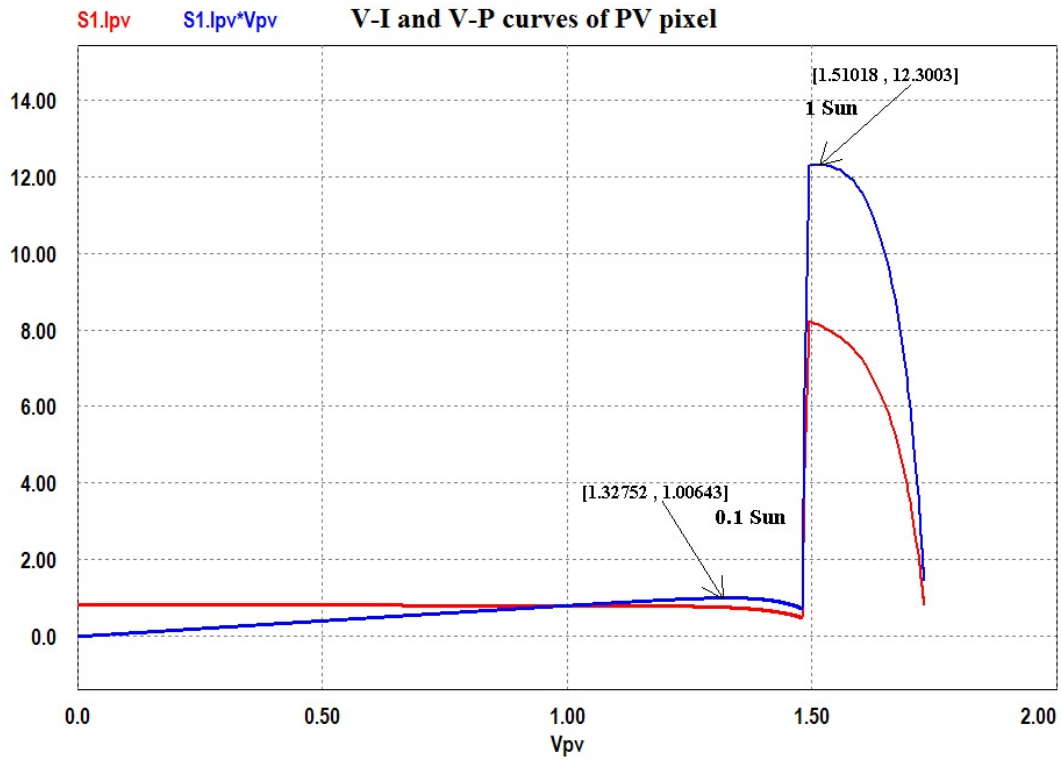


Fig. 21 V-I and V-P curves of PV pixel for step change in insolation from 0.1 sun to 1 sun

Fig. 22 below shows the pixel voltage and power for a step change in insolation. It can be seen that the MPPT algorithm effectively tracks the V-I curve of the PV pixel and operates at the MPPT voltage at a particular insolation.

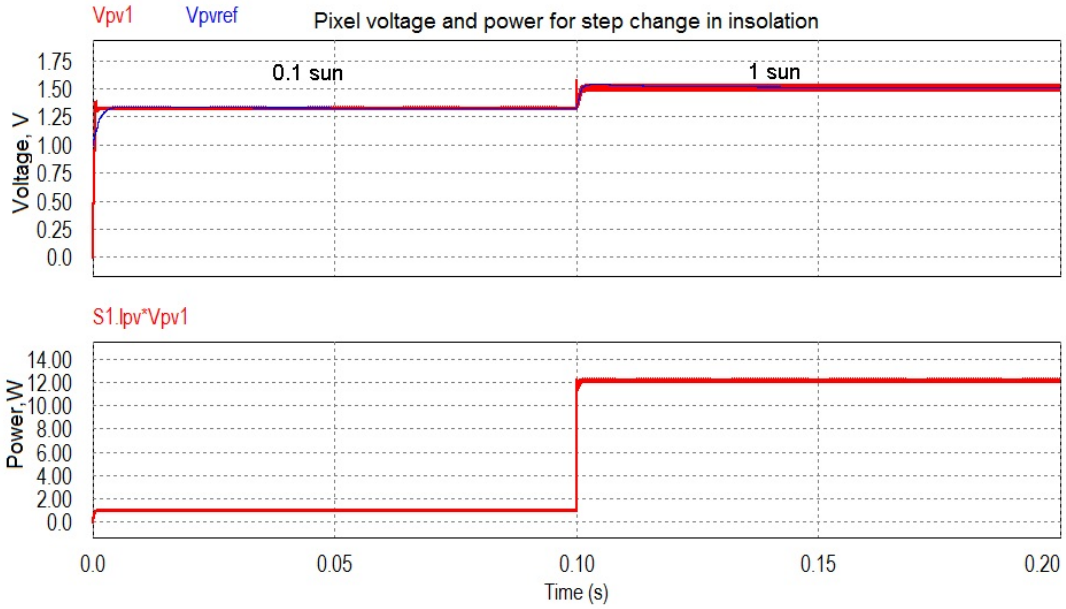


Fig. 22 Pixel voltage and power for step change in insolation from 0.1 sun to 1 sun

4.3 Control of dc-dc converters

The output voltage of the auto-connected flyback converter is based on the input pixel voltage driven by the MPPT algorithm for a particular insolation as discussed in section 4.2. The MPPT algorithm provides the reference pixel voltage, V_{ref} for which maximum power output can be obtained. This voltage is compared with the actual pixel voltage, V_{pixel} and the difference is given as an error signal to a PI controller forming the outer voltage control loop. The PI controller ensures that the pixel voltage follows the reference signal. A fast acting additional PI controller is used for the inner current control loop where the output of the first PI controller is compared with the actual output current signal. The overall control at the dc side is shown in fig. 23.

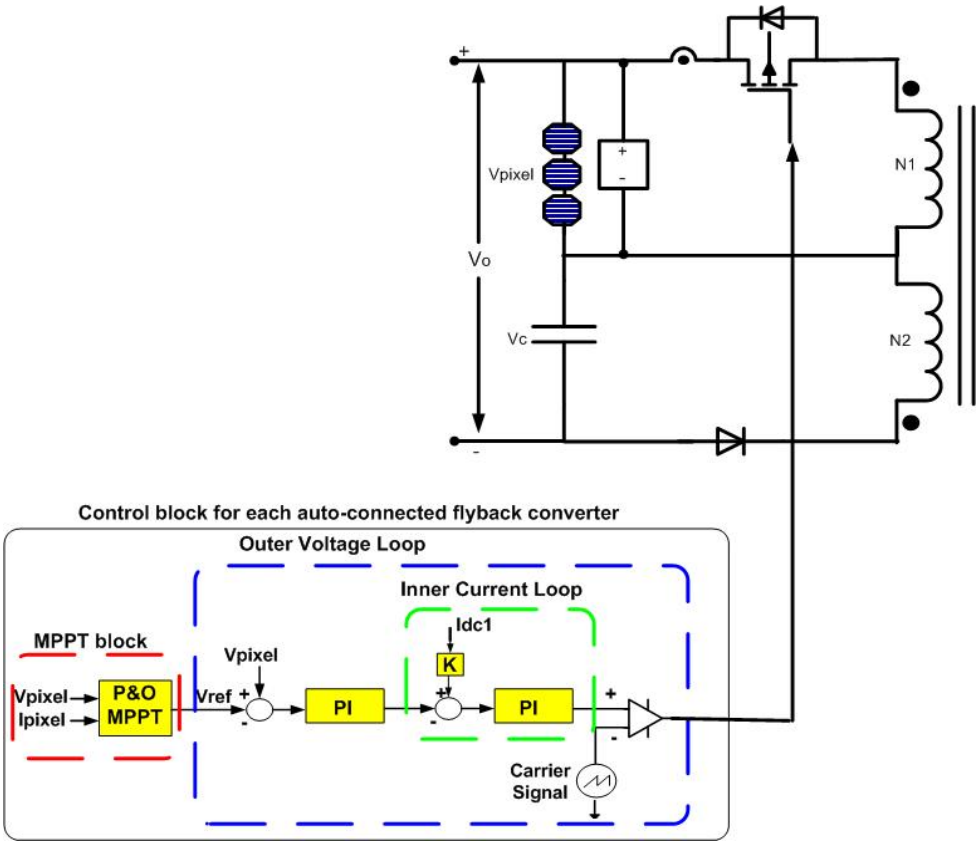


Fig. 23 Flyback converter with its control circuitry

The dc side control is accomplished by building a control circuit that varies the converter control input, duty cycle, D in such a way that the input pixel voltage, V_{pixel} is regulated to be equal to a desired reference value, V_{ref} computed by the MPPT algorithm block. In order to know how the output voltage varies with respect to the control variable, D, it is desired to obtain a model of the converters in terms of $\frac{V_o}{D}$. Hence, by small signal modeling, the required transfer function is derived using state space averaging technique [14].

The state space model of flyback converter is given by:

$$\begin{bmatrix} \dot{I}_l \\ \dot{V}_c \end{bmatrix} = A \begin{bmatrix} I_l \\ V_c \end{bmatrix} + B \begin{bmatrix} V_g \\ 0 \end{bmatrix} \quad \text{and} \quad V_o = C \begin{bmatrix} I_l \\ V_c \end{bmatrix} \tag{4}$$

On-state state matrix,

$$A_1 = \begin{bmatrix} \frac{-(r_l + r_{ds})}{L} & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \tag{5}$$

Off-state state matrix,

$$A_2 = \begin{bmatrix} \frac{-r_{dd}}{Ln^2} & \frac{-1}{Ln} \\ \frac{1}{Cn} & \frac{-1}{RC} \end{bmatrix} \tag{6}$$

Input source dependent matrix,

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{7}$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{8}$$

Output voltage matrix,

$$C_1 = C_2 = [0 \quad 1] \tag{9}$$

Equivalently, $A = A_1 D + A_2 D'$, $B = B_1 D + B_2 D'$ and $C = C_1 D + C_2 D'$ (10)

Hence, $\frac{\widehat{V_o}(s)}{\hat{d}(s)} = C(sI - A)^{-1}[(A_1 - A_2)X]$ where $X = -A^{-1} B V_g$ (11)

The open loop control-to-output transfer function is found out by using state space approach in Matlab:

$$\frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{-1881s + 2.397e7}{s^2 + 312.1s + 5.432e5}$$

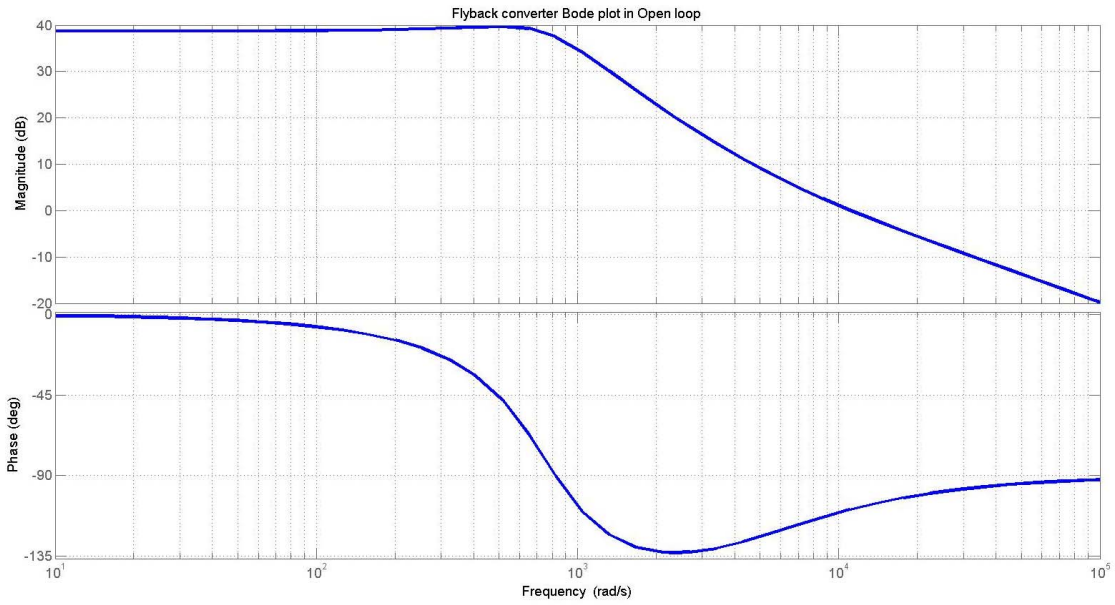


Fig. 24 Bode plot of output to control transfer function of flyback converter in open loop using state space analysis

From fig. 24 it is seen that the transfer function of the flyback converter has a zero at the RHP. The open loop output to control transfer function is also found out for the actual hardware of the auto-connected flyback converter by using the Venable analyzer. The Venable analyzer has an oscillator output which is capable of providing a dc bias voltage along with an AC voltage signal. The output of the oscillator is used as the control input which is pulse width modulated to provide the duty cycle to the converter switch. The control signal is swept from 0.1Hz to 300kHz and the bode plot

obtained is shown in fig. 25. The bode plot of the actual hardware incorporates all the parasitic involved in the circuit which is not accounted for in the state space analysis. This can be observed by the phase and magnitude plots which depict a number of parasitic poles and zeros at high frequency.

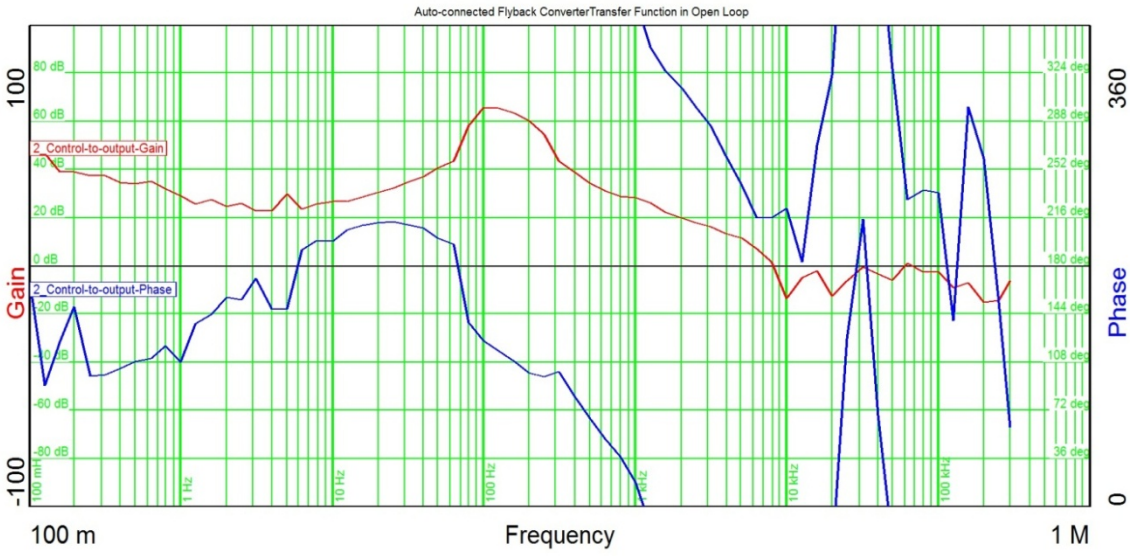


Fig. 25 Bode plot of output to control transfer function of auto-connected flyback converter in open loop using Venable Analyzer

4.4 Feed forward control of inverters

Single phase inverters suffer from a double frequency voltage ripple at the dc link [19]. The ripple in the dc link is the primary contributor for the appearance of harmonics in the inverter output not present in the PWM switching function and is therefore responsible for the deterioration in the quality of the output voltage [24]-[25]. Fig. 26 depicts the origin of the double frequency ripple in single phase voltage source inverters (VSI). For a sinusoidal output voltage and current, the AC power has a DC component and a time varying component.

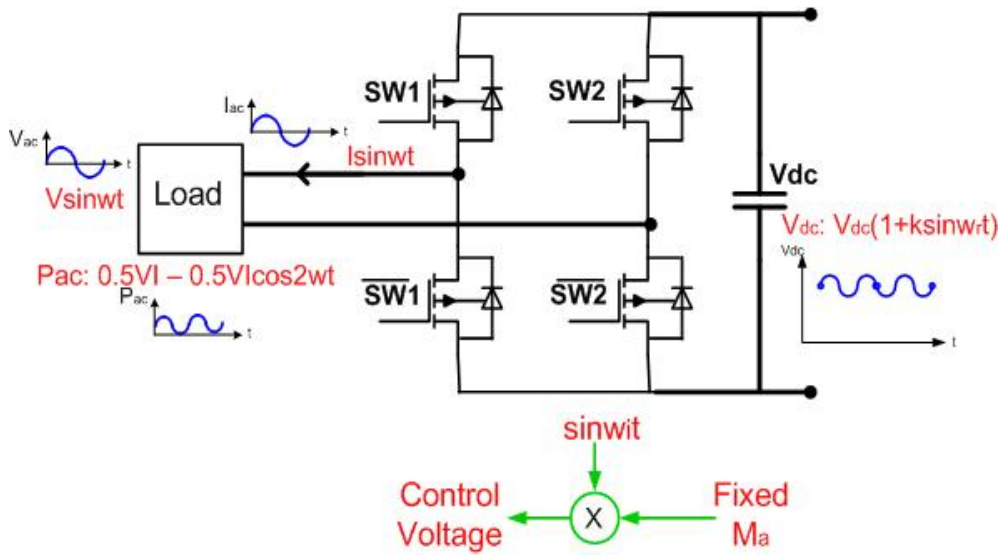


Fig. 26 Origin of double frequency ripple in single phase VSI

$$P_o = V_o sinw_i t I_o sinw_i t \tag{12}$$

$$P_o = \frac{V_o I_o}{2} - \frac{V_o I_o}{2} cos2w_i t \tag{13}$$

$$V_{dc} I_{dc} = \frac{V_o I_o}{2} - \frac{V_o I_o}{2} cos2w_i t \tag{14}$$

$$I_{dc} = \frac{V_o I_o}{2V_{dc}} - \frac{V_o I_o}{2V_{dc}} cos2w_i t \tag{15}$$

By power balance (eq. 14) at the output and dc link, it can be seen that the inverter input current is not a pure DC but has a double frequency component which leads to a voltage ripple on the dc link capacitor voltage in a single phase VSI.

Let SW_1 and SW_2 be the inverter switching functions for the inverter operating frequency, w_i

$$SW = \begin{bmatrix} SW_1 \\ SW_2 \end{bmatrix} = SW = \begin{bmatrix} \sum_{n=1}^{\infty} A_n sin\ nw_i t \\ -\sum_{n=1}^{\infty} A_n sin\ nw_i t \end{bmatrix} \quad (16)$$

Considering a dc-link voltage ripple of frequency, w_r and magnitude $kV_{dc.}$, the inverter input voltage is written as:

$$V_i = V_{dc}(1 + ksinw_r t) \quad (13)$$

The inverter output voltage with dc-link voltage ripple is obtained as:

$$V_{ab} = V_{dc}(1 + ksinw_r t)SW \quad (14)$$

$$V_{ab} = V_{dc}A_n \sin nw_i t + kV_{dc}A_n\{\cos(w_r - nw_i)\, t - \cos(w_r + nw_i)\, t\} \quad (15)$$

Thus, the inverter output voltage will face lower order harmonics such as $(w_r \mp nw_i)$ due to the dc-link voltage ripple which degrade the quality of output voltage and results in high total harmonic distortion (THD). To counteract the double frequency ripple at the dc link voltage, a feed forward control scheme is proposed to suitably alter the modulating function to reject dc link voltage ripple [24]. The working of the feed forward control is depicted in fig. 27 given below.

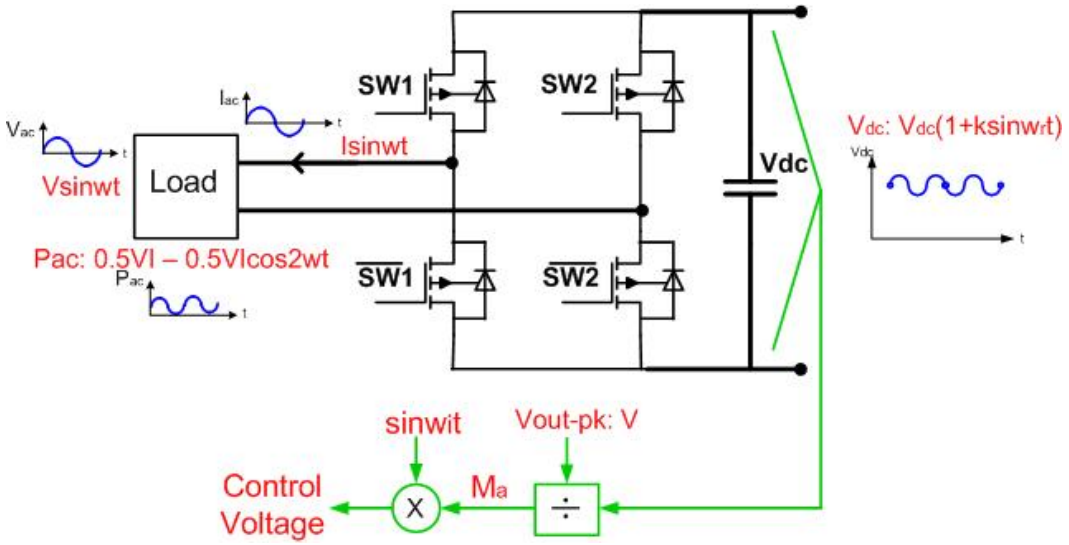


Fig. 27 Proposed feed forward control scheme

From fig. 27 it is evident that in the proposed correction scheme, the dc link voltage is sensed and the modulation function is derived by dividing the sensed voltage with the required output peak voltage. In doing so, the modulation function does not remain fixed anymore as in the case of Sine PWM where as it has the trace of the ripple voltage such as to cancel its effect at the output. The following is the mathematical analysis of the modified PWM switching function used to counter the effect of the dc-link voltage ripple:

$$SW_{new} = \frac{1}{(1+ksinw_r t)}\begin{bmatrix} \sum_{n=1}^{\infty} A_n sin\, nw_i t \\ -\sum_{n=1}^{\infty} A_n sin\, nw_i t \end{bmatrix} \tag{16}$$

$$SW_{new} = (A_1 + \frac{A_1 k^2}{2})sinw_i t - (\frac{A_1 k}{2} + \frac{3A_1 k^3}{8})\cos(w_r - w_i)t + (\frac{A_1 k}{2} + \frac{3A_1 k^3}{8})\cos(w_r + w_i)t$$

$$+ \frac{A_1 k^2}{4}\sin(2w_r - w_i)t - \frac{A_1 k^2}{4}\sin(2w_r + w_i)t \tag{17}$$

SW_{new} modifies the instantaneous value of inverter modulating signal such that lower order harmonics introduced by the dc-link voltage ripple are eliminated at the inverter output voltage. Therefore, the inverter output voltage is made immune to the presence of voltage ripple on the dc link voltage bus by using feed forward control. However, at higher inverter output voltages, there is a possibility of insufficient margin to incorporate higher instantaneous values of modulating signals [24].

The inverter modules are operated to produce AC output voltage 120V/240V. The dc link voltage fluctuates to accommodate for the change in MPPT set point for different levels of insolation on the smart PV module. However, the voltage fluctuation on the dc link bus is very small since the MPPT pixel voltage set point varies by a maximum of 0.25V from 1sun to 0.1sun. Hence, depending upon the dc-link bus voltage, the modulation index adjusts itself to ensure the desired AC output voltage.

4.5 Analysis of feed forward control

An analysis of feed forward control is performed in terms of the amount of dc link voltage ripple rejected for different modulation indexes, selection of the dc link capacitor, reliability of the overall system and voltage stress on the power electronic components. The analysis is carried out using per unit quantities for the overall system specification of 240V, 235W shown in fig. 18 using Sharp's NU-Q235F2 PV module. Per unit values are calculated for the overall system with $V_{base}: 240V, P_{base}: 235W \ and \ f_{base}: 60Hz.$

4.5.1. Upper boundary of dc link voltage ripple rejected

As seen in the above section feed forward control involves modifying the switching function to reject dc link voltage ripple. In doing so, a number of different frequencies terms such as $(nw_r \mp w_i)$ are obtained by the convolution of the original switching function with the dc link voltage with ripple. Therefore, the new overall switching function demonstrates a higher peak value than that of the original switching function. Fig. 28 indicates the modified switching function waveforms for different values of k for an original modulation index, A of 0.8. It can be seen from the figure that as the value of dc link ripple increases, the switching function starts having a more pronounced effect of the additional frequency terms making it obtain a higher peak than the original. Since, the new synthesized switching function is superimposed with the carrier triangular wave for PWM modulation, the peak of the new switching function determines the modified modulation index. This plays an important role in determining the upper boundary of the voltage ripple that can be tolerated given a particular modulation index.

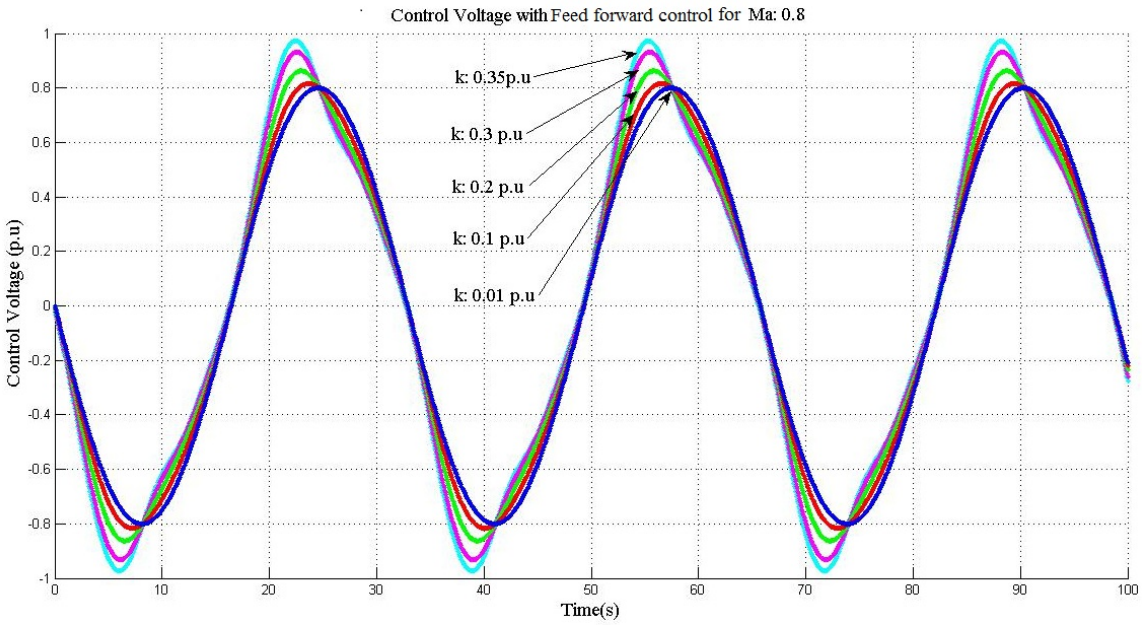


Fig. 28 Control voltage waveforms for feed forward control for Ma: 0.8

Fig. 29 elucidates that for every modified modulation index, there exists a maximum value of voltage ripple, k that can be tolerated. The maximum value of k is evaluated by the value of k for which the modified modulation index becomes one. For every value of k higher than this, the modified modulation index becomes greater than one, hence entering the zone of over-modulation. For instance, for the original modulation index of 0.8, the maximum dc link ripple that can be tolerated is 0.37p.u. (37% of dc link voltage) as at this value of k, the modified modulation index touches 1.

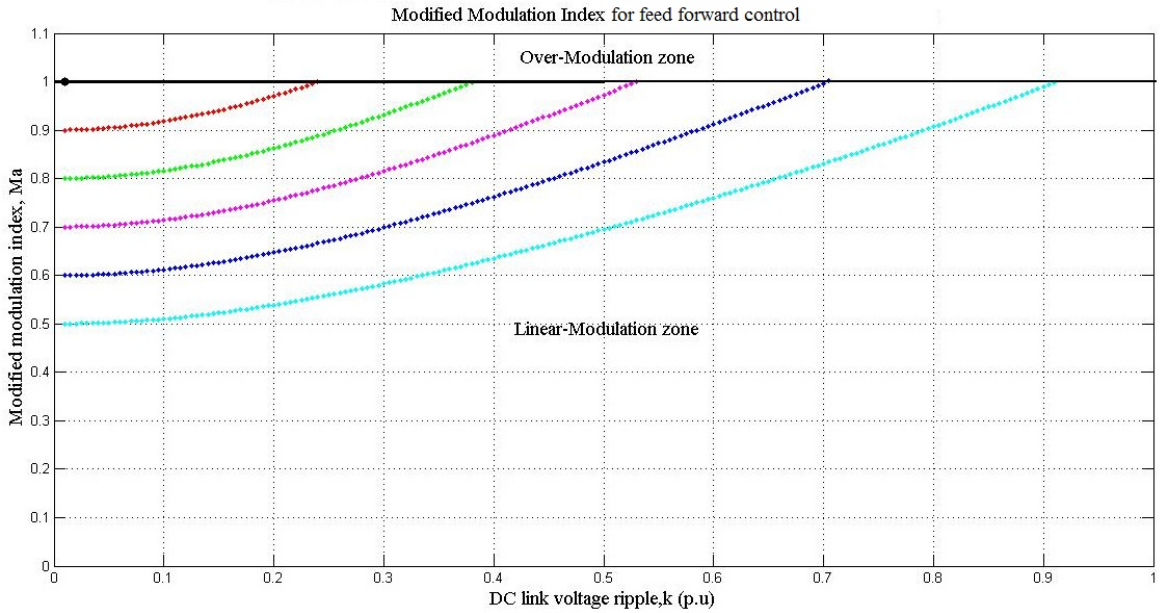


Fig. 29 Upper boundary of dc link voltage ripple rejected with feed forward control

4.5.2. Power quality analysis

Total Harmonic Distortion (THD) is a power quality measurement criterion and is defined as the summation of the harmonic components of the output current compared against the fundamental component of the output current.

$$THD = \frac{\sqrt{I_2^2+I_3^2+I_4^2+\cdots+I_n^2}}{I_1} * 100\% \quad (18)$$

$$THD = \frac{\sqrt{I_{rms}^2-I_1^2}}{I_1} * 100\% = \sqrt{\frac{I_{rms}^2}{I_1^2}-1} * 100\% \quad (19)$$

IEEE Std 519 recommends the limits on voltage harmonics to be set at 5% for THD and 3% for any single harmonic component. THD of output voltage and current with feed forward control is predicted to be low as the lower harmonic components of the output voltage are cancelled out by modifying the switching waveform as seen in

section 4.4. The modified switching function calls for a Taylor series expansion in order to eliminate the effect of the ripple present in the dc link voltage- $(1 + ksinw_r t)$. However, the entire effect of lower order terms cannot be cancelled. The output voltage waveform consists of lower order harmonics but with considerably less magnitude which overall improves the THD of the output voltage and current waveforms. Fig. 30 indicates a comparison of the THD in output current using the conventional sine switching function (SPWM) and the modified switching function obtained by feed forward control.

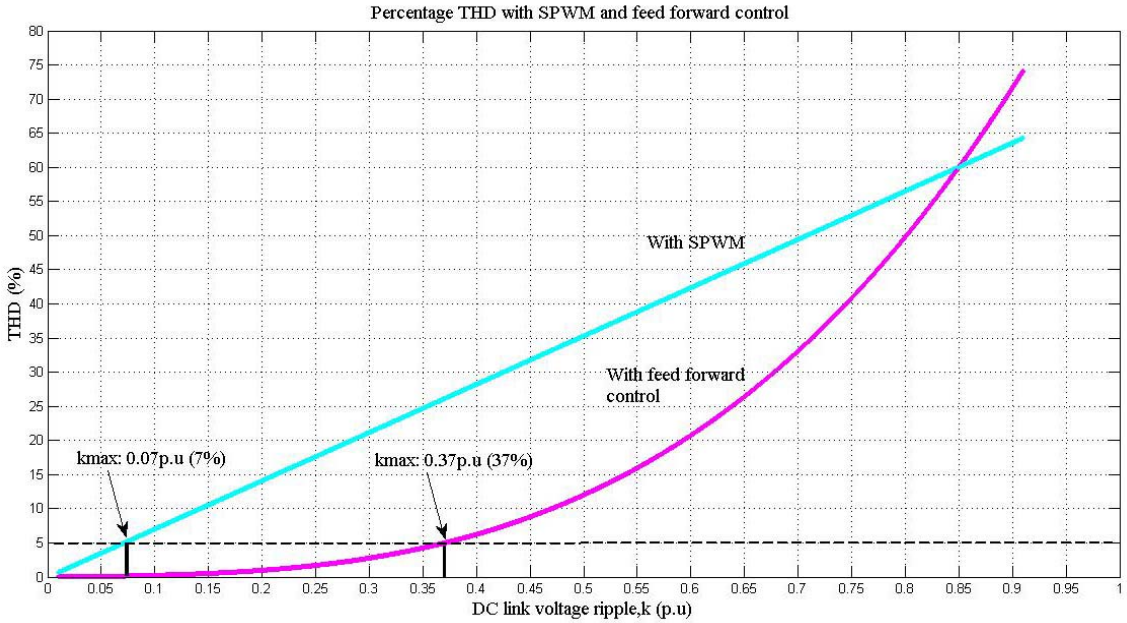


Fig. 30 Percentage THD with SPWM and feed forward control

The figure illustrates that with SPWM, a maximum of 7% dc link ripple can be tolerated, where as with feed forward control, a maximum of 37% dc link ripple can be tolerated for a THD of 5%. This proves that with feed forward control, much higher dc link ripple voltage can be sustained without compromising the output voltage and current quality.

4.5.3. DC link capacitor selection

The size of the dc link capacitor is determined by its capacitance and the maximum operating voltage. The proposed modulation technique is an incentive to reduce the value of dc link capacitance by making it endure higher ripple voltages. From the power quality anaysis in section 4.5.2 it is seen that a maximum 37% dc link voltage ripple can be tolerated for a THD of maximum 5%. Since, voltage ripple on the dc link capacitor is inversely proportional to the capacitance, the capacitance can be effectively reduced by allowing higher ripple voltages across the capacitor. The dc link capacitance equation is given by:

$$C_{dc} = \frac{P_{dc}}{2w_i k V_{dc}^2} \tag{20}$$

The value of C_{dc} is affected by the amount of dc link ripple, k and also the dc link bus voltage which decides the value of modulation index [26]-[27]. Fig. 31 shows the value of capacitance in p.u wrt dc link voltage ripple for different values of modulation index. The graph signifies that capacitance reduces considerably with the value of k until k equals 0.2 p.u (20% ripple). For values of k greater than 0.2, the reduction in capacitance is not very significant. Again, tracing back to the requirement of maximum 5% THD, it can be seen that the capacitance reduces significantly by feed forward control as compared to sine PWM. This is because with sine PWM, the maximum value of k can be 0.07p.u. (7% ripple) where as with feed forward control, the maximum value of k can be 0.37 p.u (37% ripple). Therefore, it can be inferred that feed forward control offers significant reduction in capacitance as compared to the conventional sine PWM.

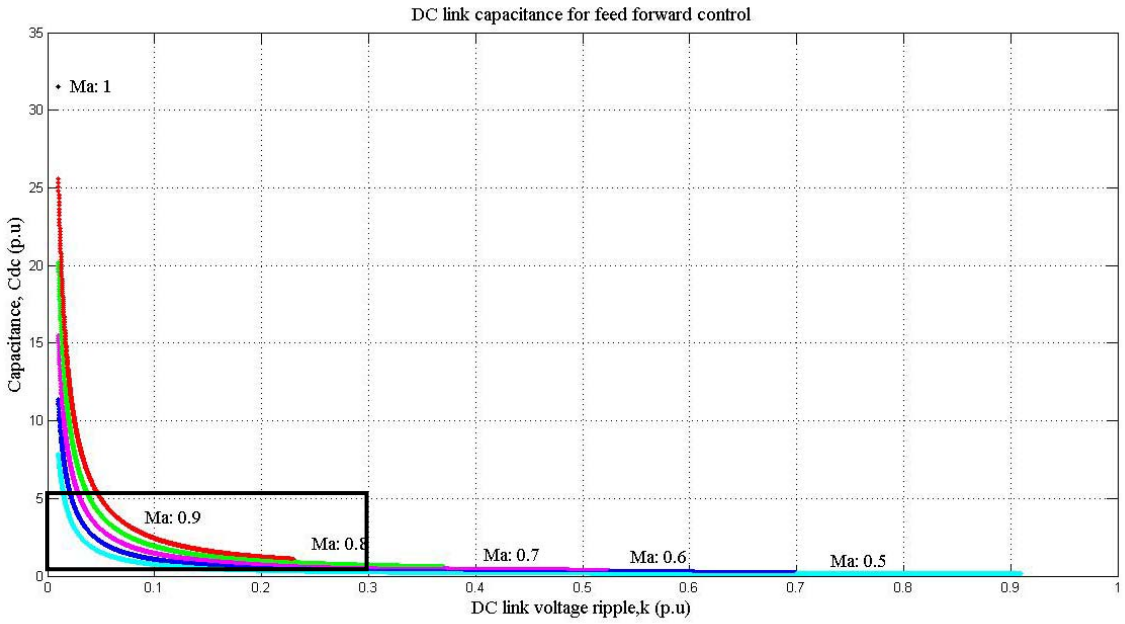


Fig. 31 DC link capacitance reduction for feed forward control

Fig. 32 shows the zoomed in view of fig. 31 with the objective of determining the effective reduction in capacitance by feed forward control. For the analysis two operating points are chosen. With SPWM, as previously established in section 4.5.2, the maximum value of k taken is 0.07 p.u. where as for feed forward control, the operating point is conservatively chosen for k = 0.2 p.u. as for values of k higher than 0.2p.u. there is not a very significant reduction in capacitance. The graph shows that for the modulation index of 0.9, the effective reduction in capacitance is approximately 1.25 p.u. which translates to 85 uF. Therefore, the reduction in capacitance by feed forward control is around three times that of the capacitance with SPWM.

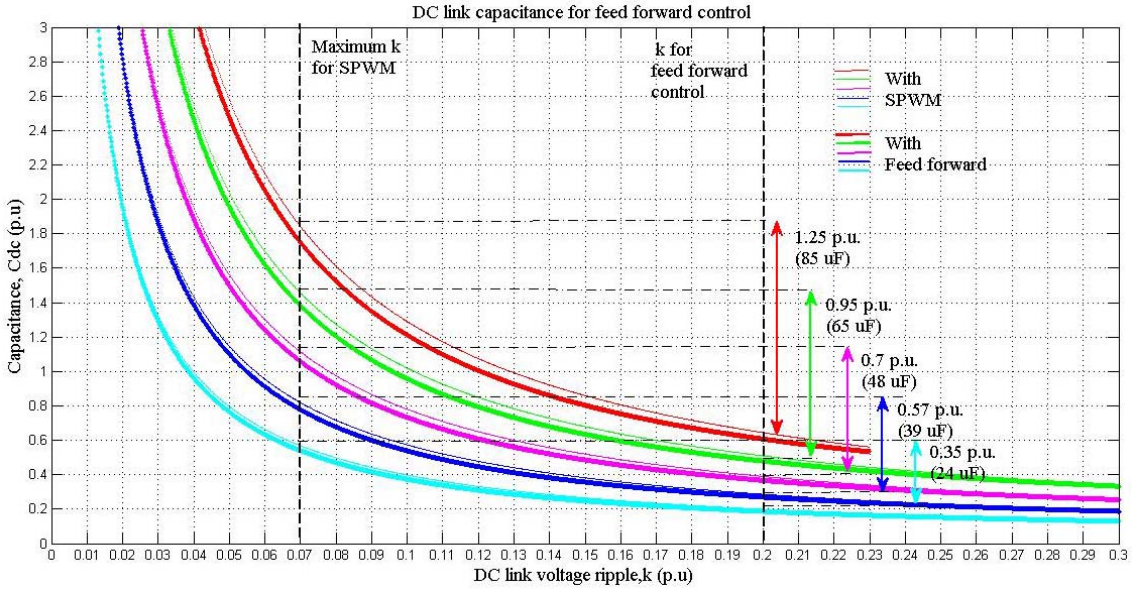


Fig. 32 Zoomed in view of dc link capacitance reduction with feed forward control

However, with the decrease in capacitance, the voltage rating of the dc link capacitor increases as the ripple on dc link bus increases. The effect on capacitor voltage rating with increase in ripple voltage can be seen in the fig. 33 for different modulation indexes. The voltage rating of the dc link capacitor is given by:

$$V_{dc-cap} = V_{dc-avg} + 0.5 * k * V_{dc-avg} \quad (21)$$

In the same way as the previous analysis on reduction in dc link capacitance, the zoomed in view of the increase in rated voltage of the dc link capacitor is shown in fig. 34 by considering the same two operating points.

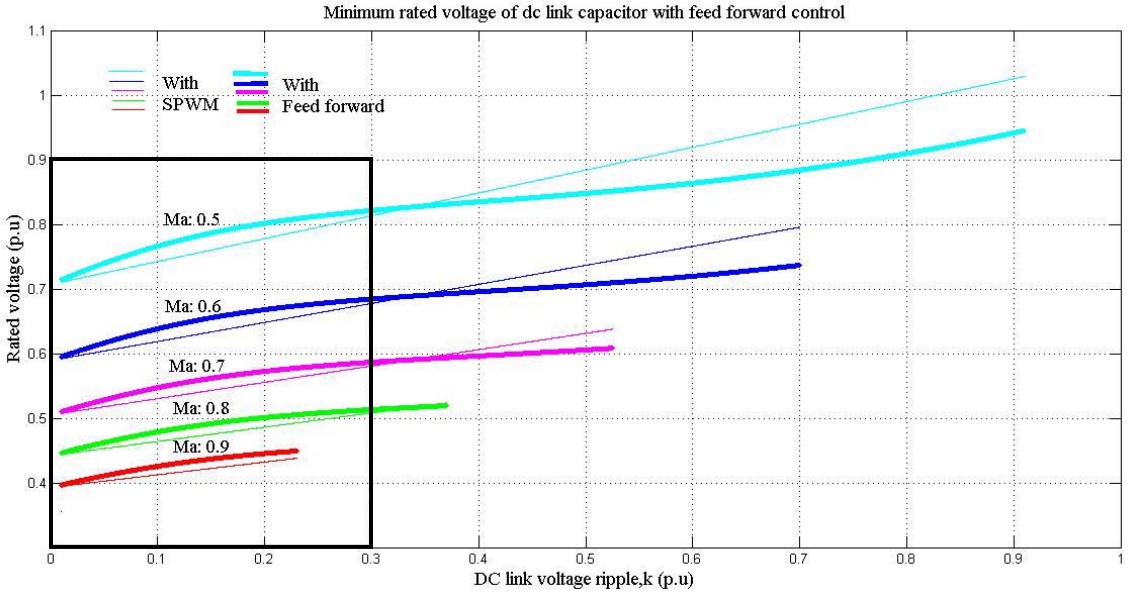


Fig. 33 Minimum rated voltage of dc link capacitor with feed forward control

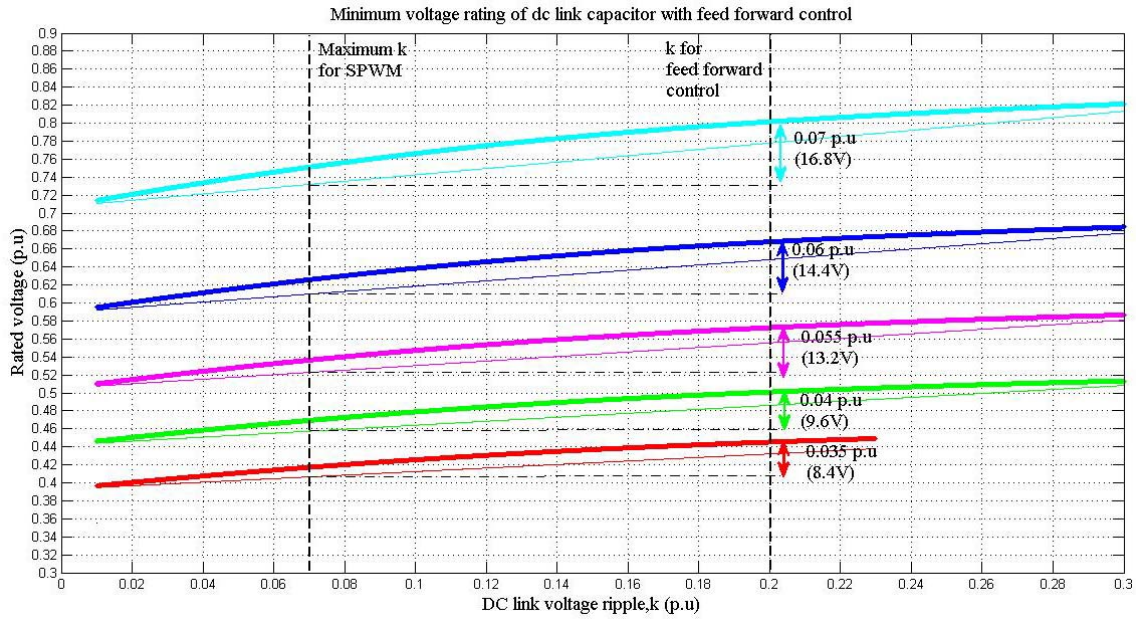


Fig. 34 Zoomed in view of minimum rated voltage of dc link capacitor with feed forward control

From the graph, it can be seen that the increse in voltage rating of the capacitor for the modulation index of 0.9 is approximately 0.07 p.u. which translates to 16.8V.

The net increase in the capacitor voltage rating by feed forward control is around 1.1 times that of SPWM.

The overall size of the dc link capacitor isdetermined by the average energy stored in it which varies with capacitance and square of the average dc link voltage seen by the capacitor.

4.5.4. Reliability improvement with film capacitors

The concept of smart PV module involves incorporating the power electronics within the PV module itself which necessitates that both the PV module and the power converter must have matched expected lifetimes so that the integrated-inverter has a lifetime that matches the PV module, namely 25 years or more [28].

Recent developments in PV cell technologies in terms of cost, efficiency and reliability have exposed power converters as the weak link in solar PV system. A study on reliability prediction for the different PV converter topologies in terms of mean time between failures (MTBF) has shown that the elctrolytic dc link capacitor has the lowest MTBF [26],[14]. The MTBF of the different power electronic components for the flyback inverter topology with electrolytic dc link capacitor shown in fig. 35 are evaluated in [28].

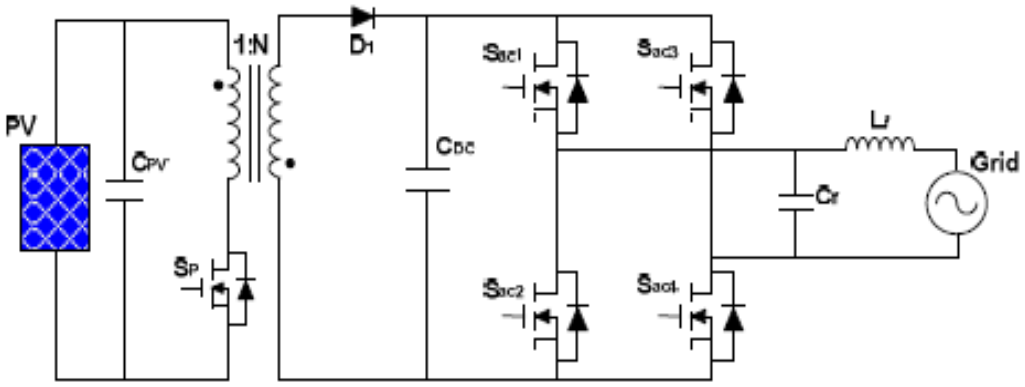


Fig. 35 Flyback inverter with electrolytic dc link capacitor taken from [28]

Table 4 MTBF of power electronic components of flyback inverter taken from [28]

Power Electronic Component	*MTBF (million hours)*
Inverter MOSFETs	169.6
Flyback diode	19.41
DC link capacitor	0.892
Transformer	41.48

Table. 4 indicates that the MTBF of the dc link capacitor is the lowest and hence decides the overall reliability of the system. Therefore, it is necessary to focus on improving the reliability of the dc link capacitor. Studies have also established that the use of film capacitors in place of the electrolytic capacitors at the dc link significantly improves the MTBF and lifetime of the overall system [28]. Fig. 36 shows the lifetime of electrolytic (L_{E_DC}) and film (L_F) capacitors used for dc link applications. It can be seen that the lifetime of film capacitors is an order higher magnitude than that of electrolytic capacitors [28].

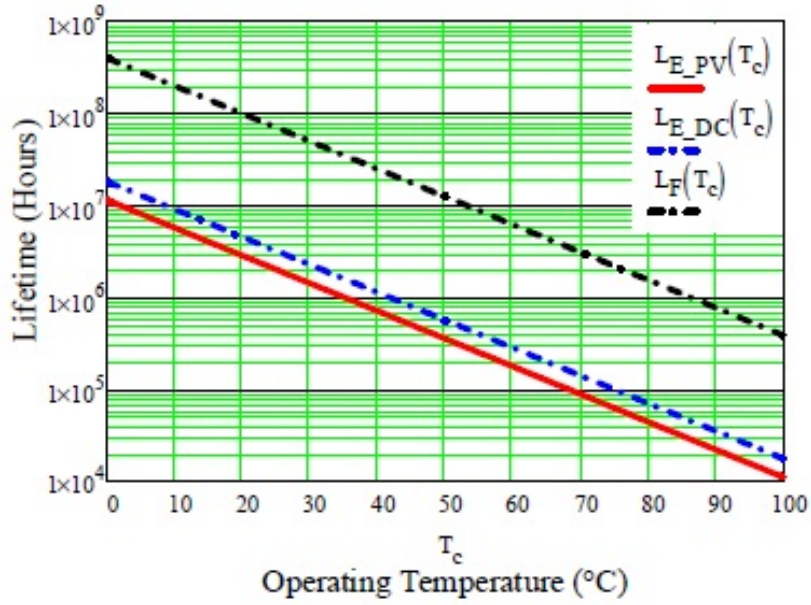


Fig. 36 Lifetime of electrolytic and film capacitors taken from [28]

Moreover, film capacitors have the following advantages as compared to the electrolytic capacitors which prompt them to be a better choice for the dc link capacitor:

- Two times voltage capability [29]
- Three times ripple current capability [29]
- Dry construction [29]
- Solid encapsulation delivers higher shock and vibration withstanding [29]
- Non-polar dielectric delivers reverse-proof mounting and AC withstanding [29]

However, film capacitors have lower energy density as compared to electrolytic capacitors which implies larger capacitor size. The energy density of electrolytic capacitors used for power electronic applications is approximately 2 J/cm^3 [30]. The energy density of film capacitors depends on the type of dielectric used. The dielectric

most often used in power electronics applications is polypropylene because it has low dissipation factor (DF) that permits high AC currents with low self heating, and it performs well over the temperature range and frequencies. The energy density of polypropylene based film capacitors is approximately 1.1 J/cm^3 [31]. At this point, it is interesting to explore the average energy stored in the dc link capacitor in order to get an estimate of the space requirement of the two capacitors.

Average energy stored in the dc link capacitor is given by:

$$E = \frac{1}{2} C_{dc} V_{dc-avg}{}^2 \tag{22}$$

The average energy stored in the dc link capacitor is then evaluated using eq. 22 for different dc link voltage ripple values for both SPWM and feed forward control and is shown in fig. 37.

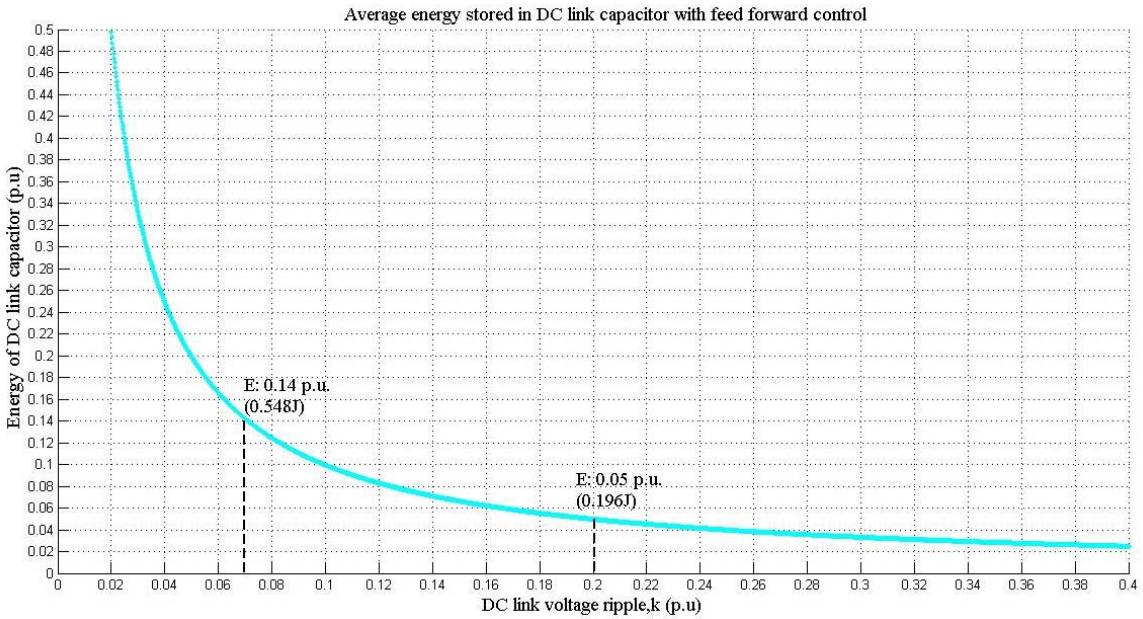


Fig. 37 Average energy stored in the dc link capacitor

It is seen from the figure that the energy stored in the capacitor is same for both SPWM and feed forward control. This can be attributed to the fact that for a particular amount of ripple, the average energy remains the same even though the average voltage and capacitance is different for both control schemes. Moreover, the average energy stored in the capacitor decreases with increase in voltage ripple because the decrease in capacitance has a more pronounced effect than the increase in average voltage. Therefore, the energy curve tends to have the same trend as the curve on reduction in capacitance shown in fig. 31. The same two operating points are chosen for the analysis as previously done- k: 0.07 p.u for SPWM and k: 0.2 p.u for feed forward control. It is found that the net reduction in energy is approximately 0.09 p.u which translates to 0.352 J. Table 5 shows an estimate of reduction in capacitor size by replacing the electrolytic capacitor used for SPWM with film capacitor used for feed forward control.

Table 5 Estimation of size of dc link capacitor

Modulation Scheme	***Capacitance, Cdc***	***Average Vdc***	***Energy stored in Cdc***	***Energy Density***	***Volume of Cdc***
SPWM (k:0.07 p.u) Electrolytic cap	129 uF	97.2V	0.6 J	2 J/cm^3	0.3 cm^3
Feed forward control (k:0.2p.u) –Film cap	41 uF	105.6V	0.22J	1.1 J/cm^3	0.2 cm^3

4.5.5 Evaluation of switch stress

The proposed modulation scheme has an effect on the voltage rating of the inverter switches and the flyback diodes as the amount of ripple endured at the dc link causes an increase in the blocking voltage. Table. 6 gives the voltage rating of the power electronic components in the system.

Table 6 Voltage stress on power electronic components

Power Electronic component	***Voltage rating (V)***
Flyback diode	$nV_{pixel} + V_{dc}/5$
Flyback switch	$V_{pixel} + V_{dc}/5n$
DC link capacitor	V_{dc}
Inverter switches	$V_{dc}/2$

Fig. 38 given below shows the per unit variation in voltage rating for the power electronic components namely flyback diode, flyback switch and the inverter switches. The voltage rating of the inverter switches is maximum as each of the inverter switch is rated for half the dc link voltage. The voltage rating of the flyback diodes are also affected by the dc bus voltage but has a reduced effect due to the series connection of the converters.

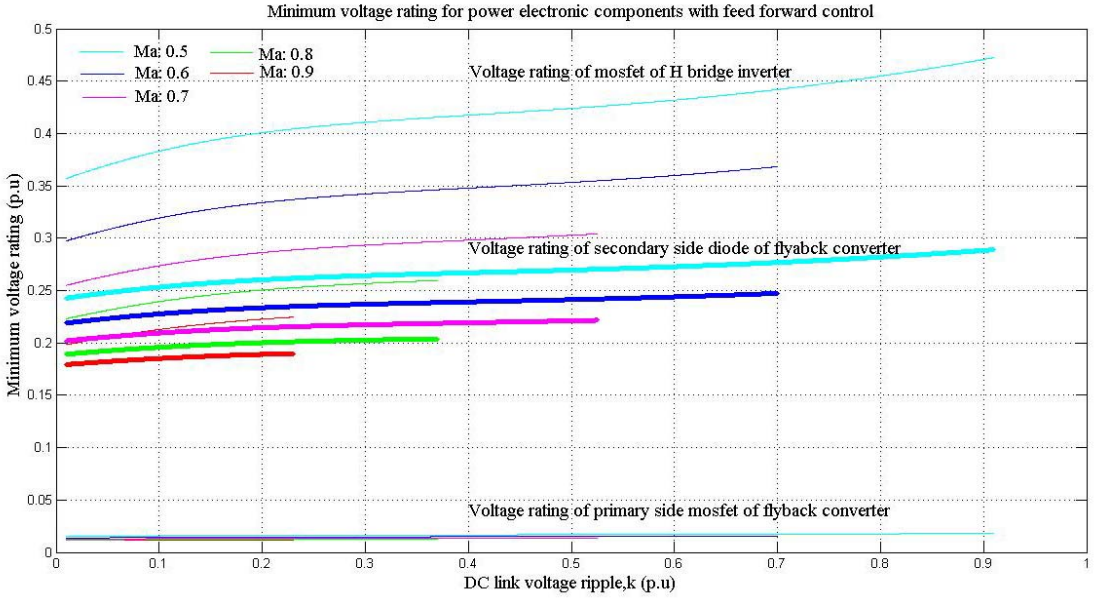


Fig. 38 Voltage rating of power electronic components with feed forward control

4.6 Conclusion

The overall control of the smart PV module has been explained. Perturb and Observe MPPT algorithm has been chosen and its implementation has been discussed followed by the control of the flyback converters. A feed forward control scheme has been proposed for the control of inverters in order to reject dc link voltage ripple. An analysis of the proposed control technique shows that the size of the dc link capacitors can be reduced, system reliability can be improved by the replacement of the dc link electrolytic capacitors with film capacitors.

5. DESIGN OF SMART PV MODULE

5.1 Introduction

The effectiveness of the proposed concept of smart PV module is demonstrated by simulation results and experimental hardware results for a design example. The design is carried out for the output voltages of 120V and 240V AC for the overall system power architecture explained in section 3.

5.2 Design example

The electrical specifications for Sharp's NU-Q235F2 PV module are given in table.7

Table 7 Module specification for Sharp's NU-Q235F2 module

Module Specifications	*Ratings*
Maximum Power	235W
Type of Cell	Monocrystalline Silicon
Cell Configuration	60 in series
Open Circuit Voltage	37.0V
Maximum Power Voltage	30.0V
Short Circuit Current	8.6A
Maximum Power Current	7.84A

Choosing the power configuration to be 3 cells/ pixel and 20 pixels/module, the electrical specifications for each pixel are recomputed in table. 8.

Table 8 Pixel specifications for smart PV module

Pixel Specifications	*Ratings*
Maximum Power, P_{pixel}	11.75W
Number of cells/ pixel, n	3 in series
Maximum Power Voltage, V_{pixel}	1.5V
Maximum Power Current, I_{pixel}	7.84A

For the overall system output voltages of 120V/ 240V, the system specifications are given in table. 9

Table 9 System specifications for smart PV module

System Specifications	*Ratings*
Flyback switching frequency, f_{dc}	200kHz
Inverter switching frequency, f_{ac}	20kHz
Inverter operating frequency, f_i	60Hz
DC link voltage ripple, r	20%
DC link voltage, V_{dc}	85-100V
Output voltage of flyback converter, V_o	20V

From fig.18, the dc stage consists of five auto-connected flyback converters connected in series to form the dc link for each subsection. Each flyback converter is connected to one pixel. The voltage gain of each flyback converter is given by:

$$\frac{V_o}{V_{pv}} = \frac{DN_2}{D'N_1} + 1 \tag{23}$$

The transformer turns ratio, $N_1 : N_2$ is selected to be 1:16 in order to incorporate for losses and maintain high output voltage at reduced insolation. The duty ratio is found out to be D: 0.435.

Given an input current ripple, Δi_l 5%, the magnetizing inductance of the flyback transformer is calculated by considering a maximum duty ratio, $D_{\max}$: 0.7 and I_{pk}: 16.5A at 1 sun [32].

$$L_m = \frac{(V_{pixel} D_{\max})^2}{P_{pixel} f_{dc}} \left(\frac{I_{pk}}{\Delta i_l} - 0.5\right) = 7.35\ \mu\text{H} \tag{24}$$

Output capacitor for flyback converter is given by:

$$C_o = \frac{P_{pixel} D}{V_o \Delta V f_{dc}} = 1.05\ \mu\text{F} \tag{25}$$

The dc link capacitance is determined by the energy stored in the capacitor and the voltage ripple tolerated. The overall power at the dc link bus is the sum of the power produced by each pixel. To find the maximum capacitance, each pixel is considered to operate at 1 sun, producing P_{dc}: 58.75W for five series connected pixel-flyback converter blocks. For a dc link voltage ripple of 20%, k is 0.2. ΔV_{dc} is given by kV_{dc}.

$$C_{dc} = \frac{P_{dc}}{2w_i V_{dc} \Delta V_{dc}} = 45\mu F \tag{26}$$

The filter inductor is given by:

$$L_{ac} = \frac{0.05 * V^2}{P 2\pi f_i} = 16 \text{ mH} \tag{27}$$

5.3 Simulation results

The overall system level simulations for 3 cell/ pixel configuration of Sharp's NU-Q235F2 PV module are performed in Psim environment for the design example explained in the previous section. Fig. 39 shows the overall system simulation schematic in Psim.

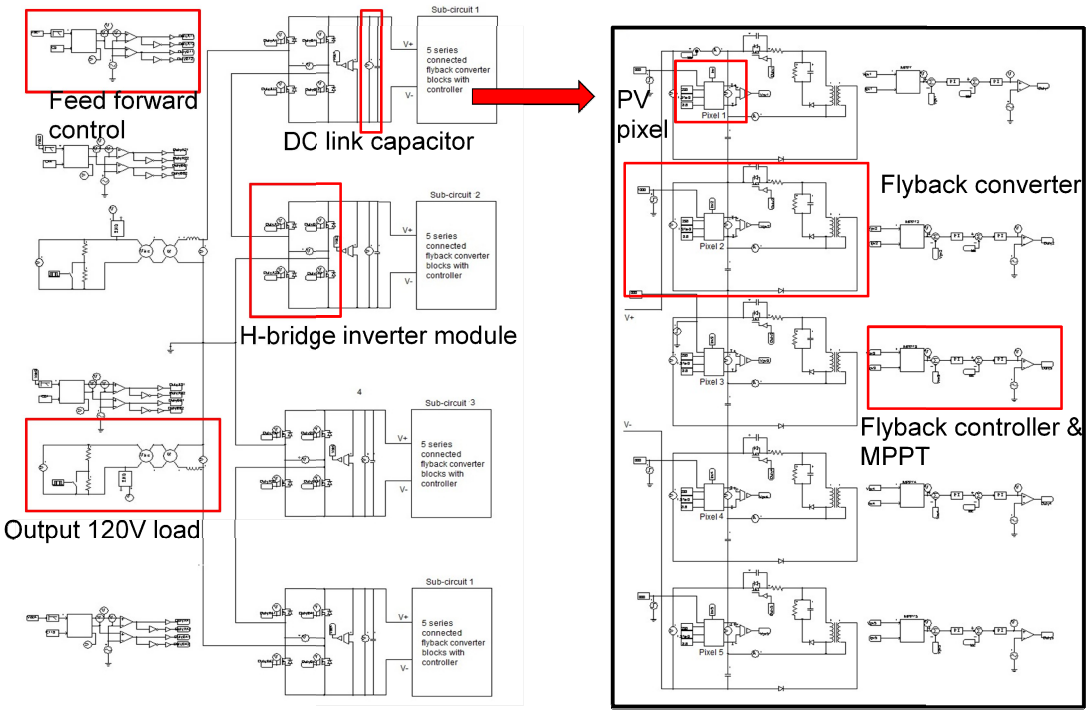


Fig. 39 Overall system simulation schematic in Psim

A step change in insolation from 1 sun to 0.5 sun is implemented at time : 0.2s. The power produced by the smart PV module thus falls from 235W to 117.5W. At the same time as the change in insolation, the value of load resistance is also doubled so that the output current reduces by half for the reduced insolation without affecting the output voltage. Fig. 40 elucidates the output load voltages of 120V rms and the floating output voltage of 240V rms obtained by adding the two inverter output voltages. Moreover, the output current reduces by half due as the power produced by the smart PV module reduces to half. The dc link voltage required for producing the 120V rms output voltages is also shown. As the insolation reduces, the net bus voltage produced also reduces slightly as the pixel voltages have now reduced for 0.5 sun. The dc link voltages have the 120Hz ripple as discussed in the previous sections. The dc link voltage ripple is

approximately 20% of the average dc link voltage at 1 sun as the dc link capacitors are designed for 20% ripple rejection. However, when the insolation reduces to 50%, the power produced by the smart PV module also reduces to 50% thus rendering the dc link capacitors to be oversized. Therefore, it is observed that the magnitude of ripple sustained at the dc link voltage bus also reduces by almost half.

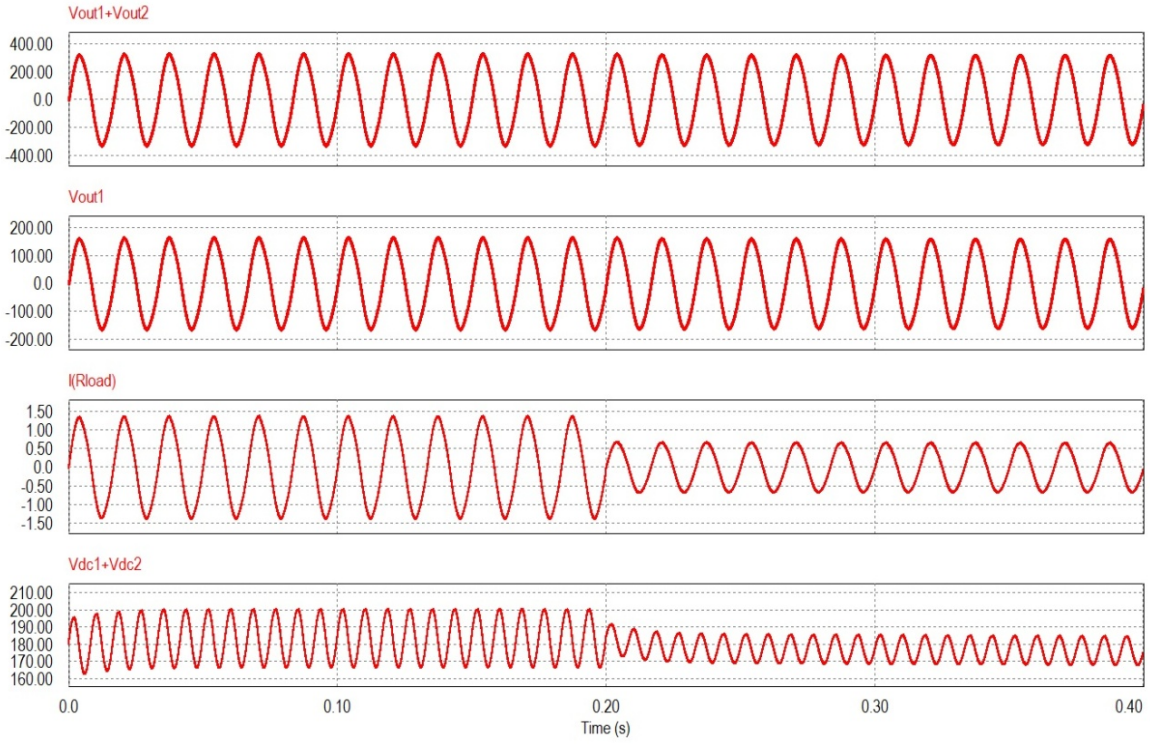


Fig. 40 System simulation: Output voltages, output current, dc link voltages

Fig. 41 illustrates the dc link voltage, V_{dc1} for one inverter module. The modified modulation index, M_{a1} with feed forward control is also shown. It is observed that the modified modulation index falls when the instantaneous dc link voltage is at a peak value whereas it saturates at 0.9 when the dc link voltage is at a minimum value. The maximum Ma of 0.9 ensures that all times, atleast 20% of the voltage ripple is rejected

as established from the analysis of upper boundary of dc link voltage ripple tolerated for different values of modulation indexes in section 4.5.1. When the insolation is down to 0.5 sun, the modified modulation index remains at the maximum value of 0.9 to signify the reduction in the dc link bus voltage. Finally, the control voltage, V_{c1} generated by feed forward control is also shown.

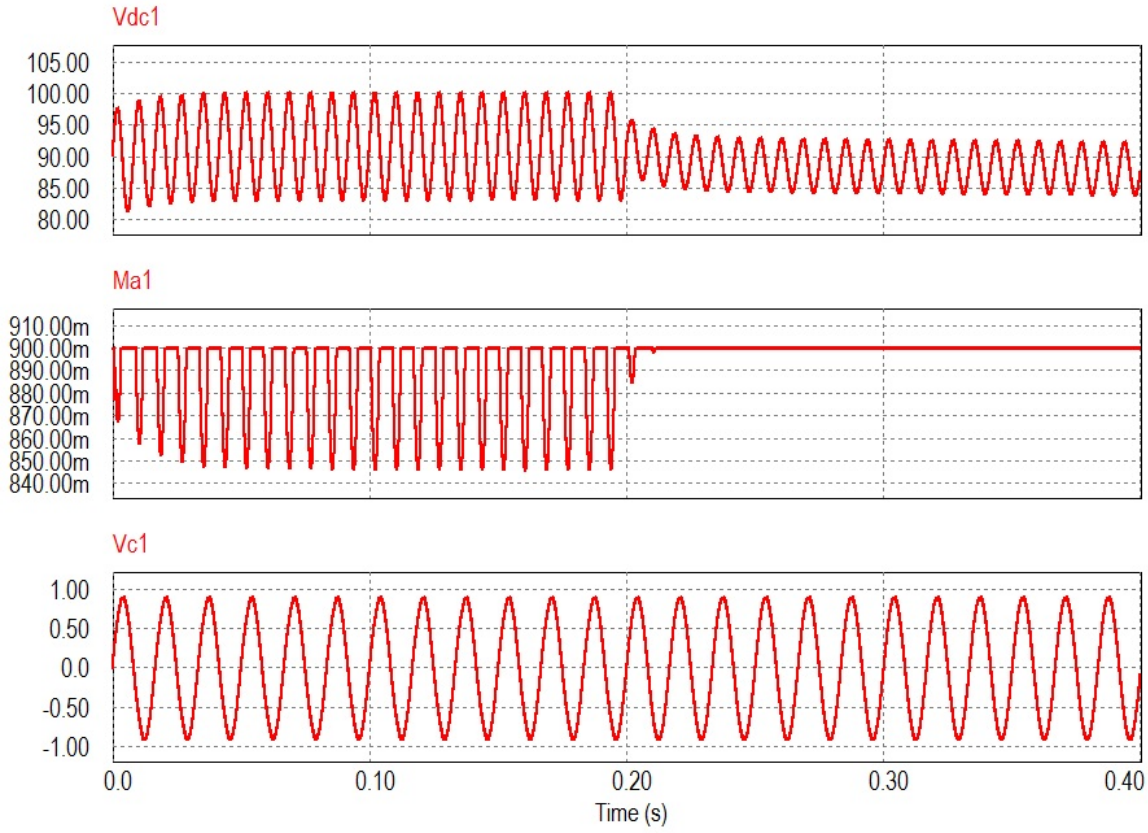


Fig. 41 System simulation: dc link voltage for one inverter, modified modulation index and control voltage for PWM of inverter

Fig. 42 shown below elucidates the change in output power and the input power for a step change in isolation. As the system is designed for two 120V output voltages, each of the 120V load resistors are rated for one half of the overall system power output.

Therefore, as the module is rated for 235W at 1 sun, the output power, W_1 for one load resistor should be 117W. However, due to parasitic resistances incorporated in the simulation model, a little less than 117W is transferred at the output.

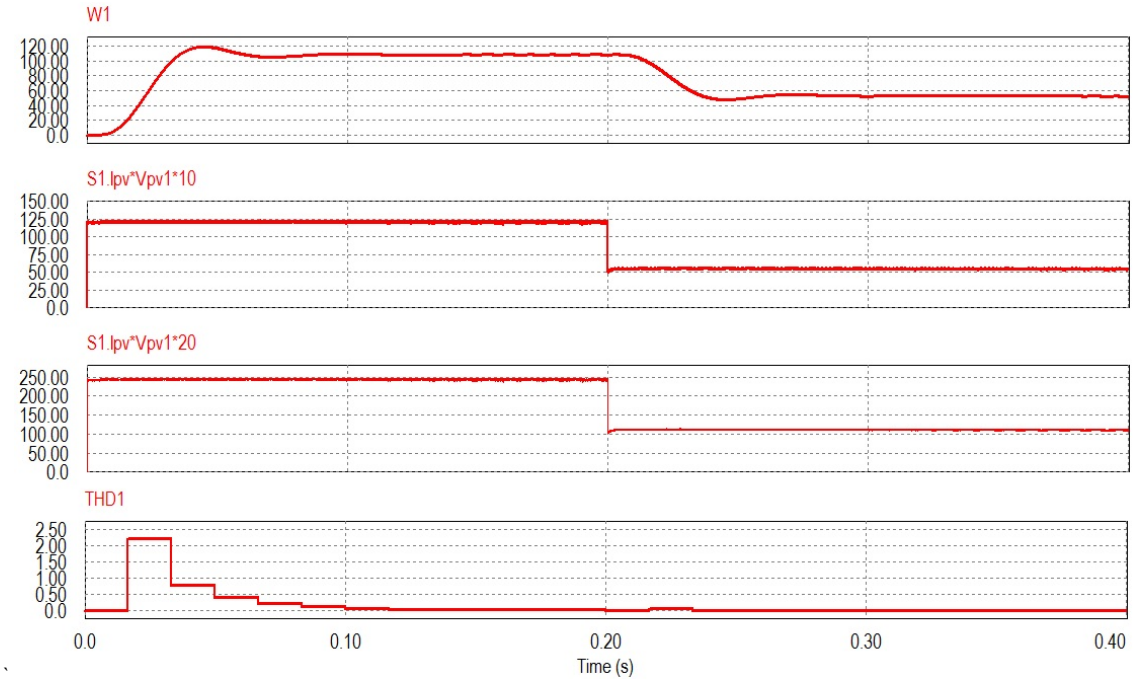


Fig. 42 Output power, pixel power and THD of output load current

The pixel power associated with producing the 120V output is also shown by the graph $I_{pv}*V_{pv}*10$. Here, the pixel power of one pixel is multiplied by 10 as there are 20 pixels in the overall system and 10 pixels are associated for producing one half of the power output. Consequently, $I_{pv}*V_{pv}*20$ gives the overall system pixel power. As the insolation reduces to 50%, the pixel power reduces to 50% as well. The graph for total harmonic distortion for output load current is also shown by THD1. It can be seen that the THD is well below the permissible limit of 5% as expected from the power quality analysis in section 4.5.2.

Fig. 43 shows the FFT of the output voltage, load current, dc link voltage and the control voltage. As predicted from the analysis, the output voltage and current are relieved from lower order harmonics however, there is still a small insignificant amount of 180Hz component which comes out to be 1.7% of the fundamental component. Therefore, it can be concluded that feed forward does not eliminate the lower order harmonics completely but reduces them significantly. From the FFT of the control voltage it is noticed that it predominantly have the 60Hz and 180Hz component for dc link ripple rejection.

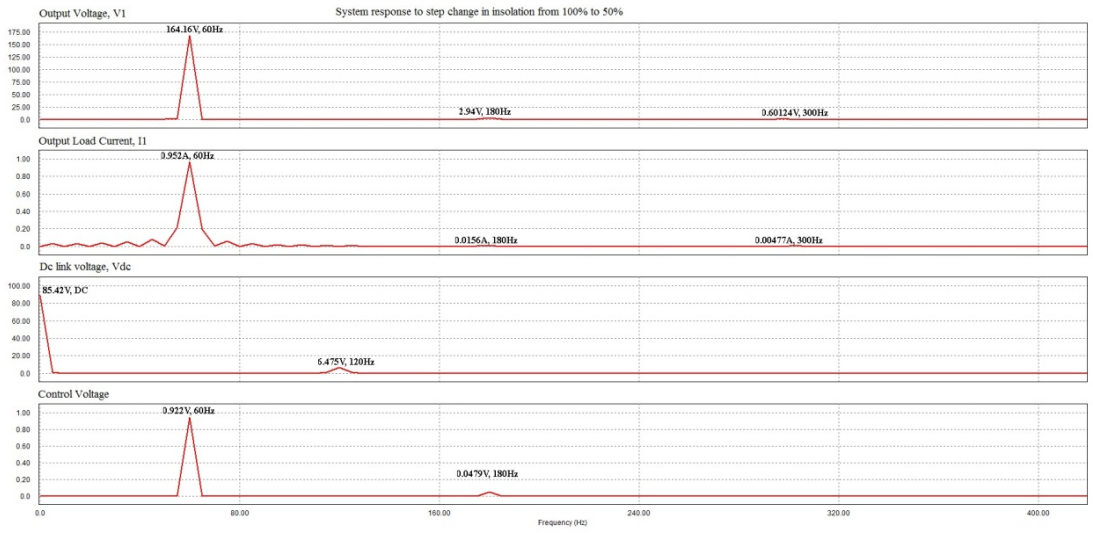


Fig. 43 FFT of output voltage, current, dc link voltage and control voltage

5.4 Experimental hardware

The laboratory prototype for smart PV module is built to validate the proposed concept of smart PV module. The auto-connected flyback converter with its associated control circuitry is designed and fabricated on printed circuit board (PCB) using Altium Designer software. A flyback transformer with magnetizing inductance 7.35μH and

turns ratio, 1:16 is designed for the prototype board [33]-[36]. The schematic of the auto-connected flyback converter along with its control and gate drive circuitry drawn using Altium Designer is shown in fig. 44.

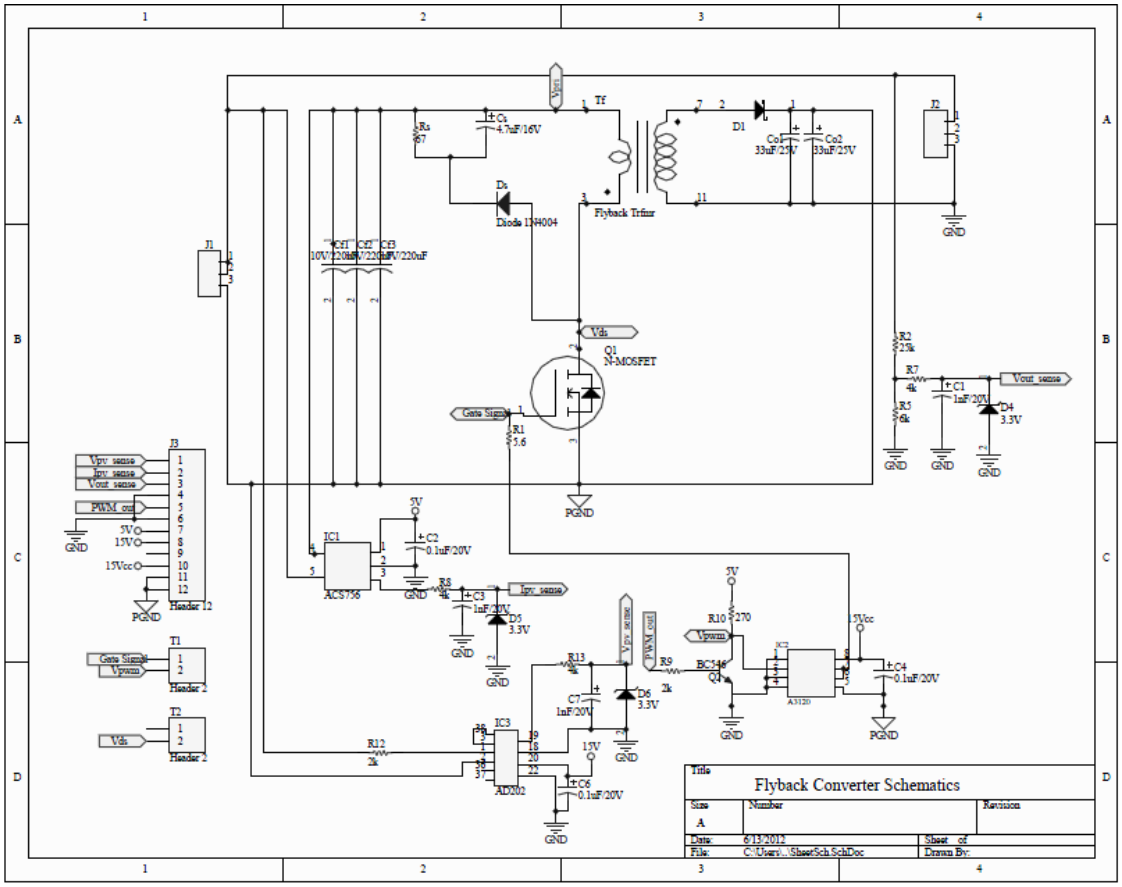


Fig. 44 Auto-connected flyback converter schematic

The power configuration of three cells per pixel serves as the input to the flyback converters. TI DSP Piccolo- TMS320F28035 is used for the digital control. Fig. 45 shows two pixels with three solar cells connected in series to form a pixel and the flyback converter required for each pixel. It can be seen that the size of the converter is much smaller than the pixel itself. However, the size of the converters can be further

reduced by a significant amount by using precise components and designing the system for higher frequency operation.

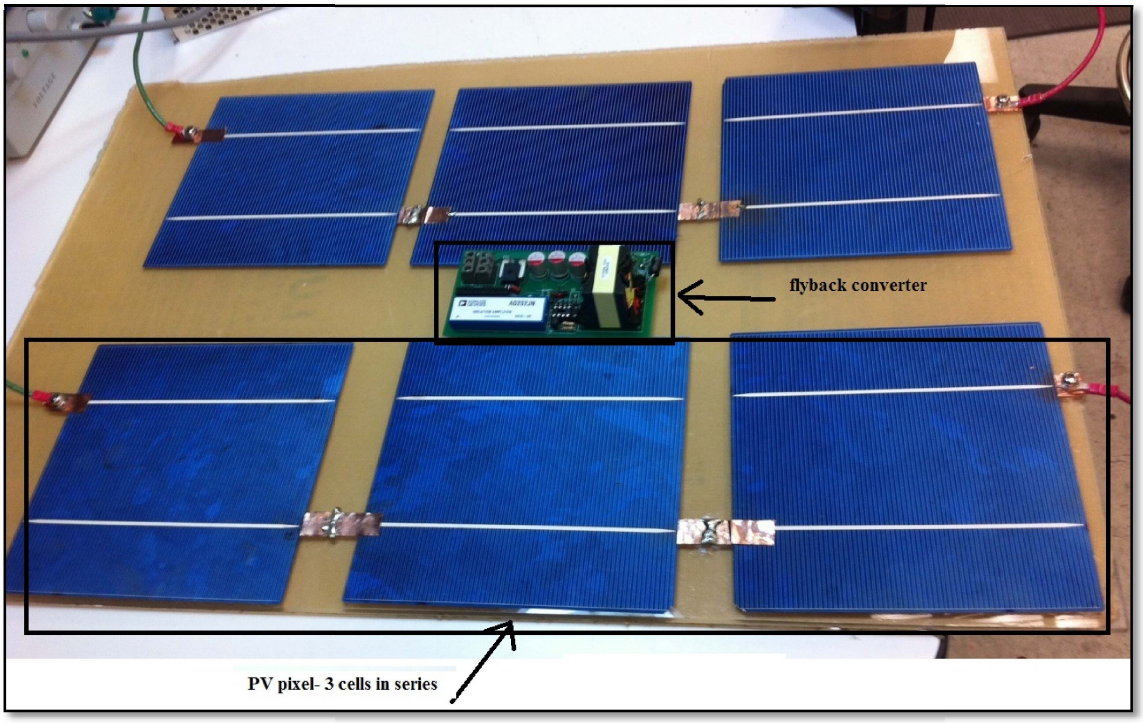


Fig. 45 Experimental hardware of pixel and converter

Fig. 46 shows the flyback converter module for each pixel. Each converter is capable of producing approximately 20- 22V output. The output of the flyback converters are then connected in series to form the dc voltage required for the operation of the inverter.

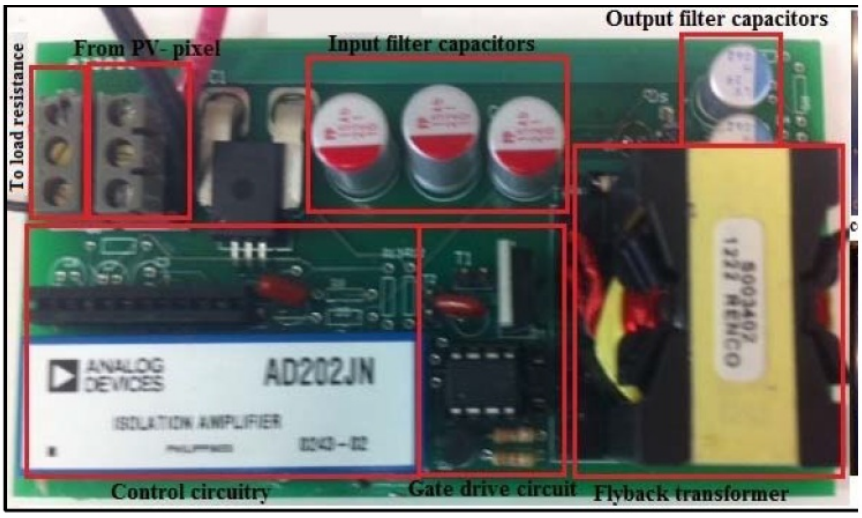


Fig. 46 Experimental hardware of auto-connected flyback converter

5.5 Experimental results

The experimental hardware prototype is tested in both open loop and with the PV pixels. The hardware results are summarized below:

5.5.1 Operation in open loop

The auto-connected flyback converter is tested in open loop using a power supply. The voltage input is set at 1.5V and a load resistor of 100 ohms is used for a power output of 4W. The duty cycle is set at 50%. The graph shown in fig. 47 shows the input voltage and the output voltage obtained from the converter.

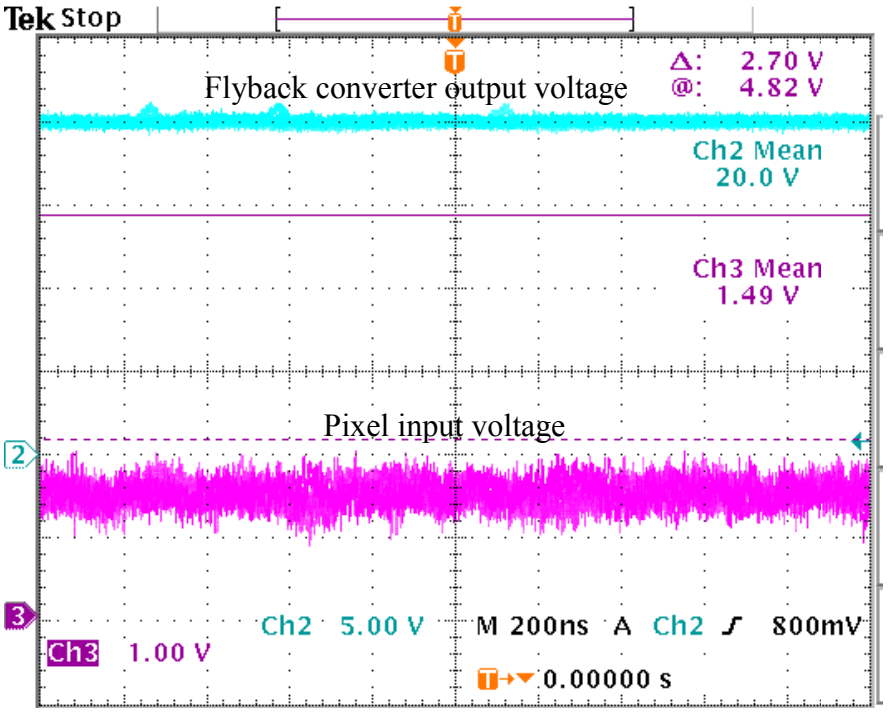


Fig. 47 Open loop: output voltage and input voltage

5.4.2 Operation in closed loop

The auto-connected flyback converter is then tested in closed loop using the PV pixel voltage as input to the converter. As the PV pixel is illuminated by using lamps in the laboratory environment, the power produced is very less. The short circuit current of the pixel is measured to be 220mA and the open circuit voltage is measured to be 1.4V. The closed loop operation of the dc-dc converter requires the MPPT algorithm. However, the MPPT algorithm requires sensing the pixel voltage and current. Since, the short circuit current produced by the pixel was very low, the current amplifier (ACS-756 rated for 50A) was not able to accurately measure the current causing an error in the MPPT algorithm. Therefore, the maximum power point was manually tracked by giving different values of duty cycle. The maximum power voltage was observed to be 1.1V

and maximum power current was observed to be 150mA. Now, for the closed loop operation, the voltage reference for pixel voltage was given as 1.1V and a PI controller was used to generate the required duty cycle. A load resistance of 1 kohms was used to obtain an output voltage of 12.84V for a maximum power of 165mW. Fig. 48 shows the pixel voltage, converter output voltage and the duty cycle.

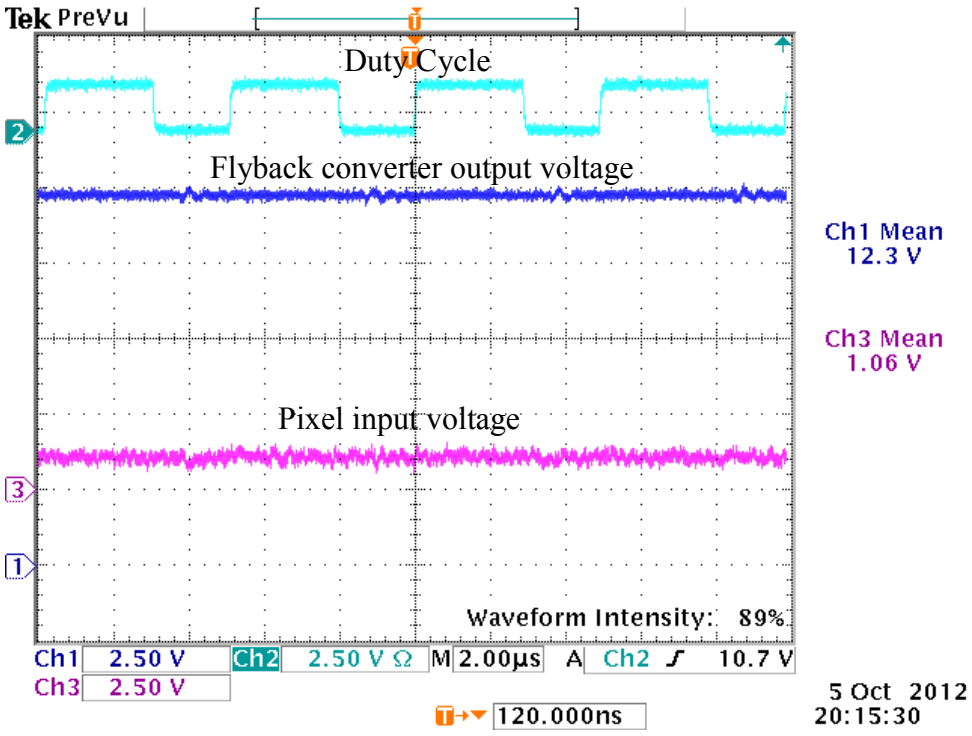


Fig. 48 Closed loop- output voltage, pixel voltage and duty cycle

Fig. 49 shows the drain to source voltage of the mosfet and the diode. When the mosfet is conducting, the diode blocking voltage is approximately 25V and when the mosfet is turned off, the diode conducts. The blocking voltage of the mosfet is approximately 1.8V.

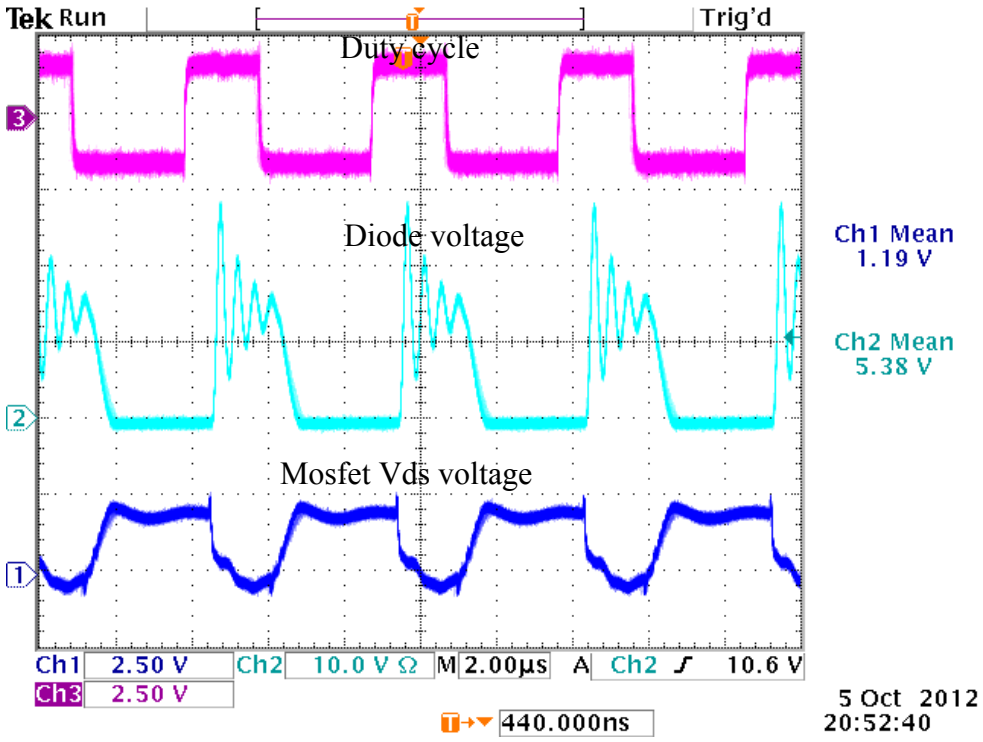
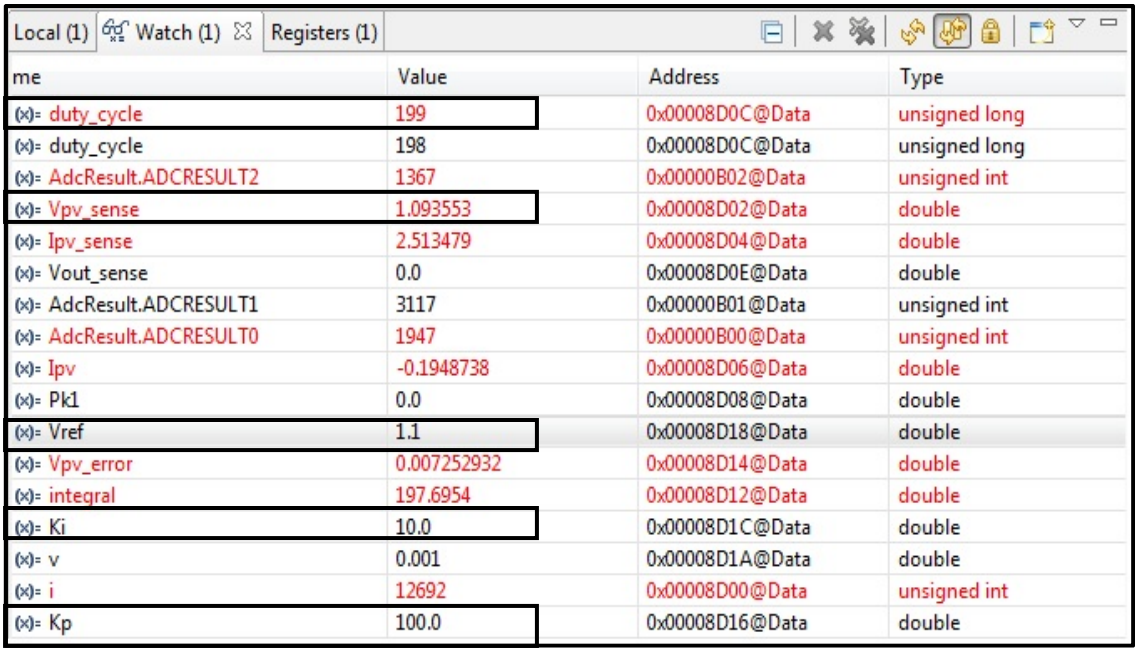


Fig. 49 Closed loop- Mosfet voltage and diode voltage of flyback converter

Fig. 50 shows the snapshot of the watch window in code composer studio (CCS4) used as a platform to code the DSP. The watch window indicates the instantaneous values of the sensed voltage and the duty cycle. The Kp and Ki values are adjusted at the watch window for real time control.



Local (1) | Watch (1) | Registers (1)

me	Value	Address	Type
(x)= duty_cycle	199	0x00008D0C@Data	unsigned long
(x)= duty_cycle	198	0x00008D0C@Data	unsigned long
(x)= AdcResult.ADCRESULT2	1367	0x00000B02@Data	unsigned int
(x)= Vpv_sense	1.093553	0x00008D02@Data	double
(x)= Ipv_sense	2.513479	0x00008D04@Data	double
(x)= Vout_sense	0.0	0x00008D0E@Data	double
(x)= AdcResult.ADCRESULT1	3117	0x00000B01@Data	unsigned int
(x)= AdcResult.ADCRESULT0	1947	0x00000B00@Data	unsigned int
(x)= Ipv	-0.1948738	0x00008D06@Data	double
(x)= Pk1	0.0	0x00008D08@Data	double
(x)= Vref	1.1	0x00008D18@Data	double
(x)= Vpv_error	0.007252932	0x00008D14@Data	double
(x)= integral	197.6954	0x00008D12@Data	double
(x)= Ki	10.0	0x00008D1C@Data	double
(x)= v	0.001	0x00008D1A@Data	double
(x)= i	12692	0x00008D00@Data	unsigned int
(x)= Kp	100.0	0x00008D16@Data	double

Fig. 50 Watch window for the closed loop control of the flyback converter

5.6 Conclusion

A design example has been provided to elucidate the concept of smart PV module. Simulation results for a step change in insolation have been shown to validate the concept. Experimental hardware aspects have also been discussed and hardware results have also been provided.

6. CONCLUSION

6.1 Summary

Solar photovoltaic plays an important role in the renewable energy domain. With the growing PV sector, it has become crucial to focus on the power conditioning for solar PV. The power conditioning unit required for a solar PV system depends upon the scale of deployment, requirements such as efficiency, reliability, flexibility and control.

A literature review of the past, present and future power conditioning unit topologies was carried out in section 2. A comparison of the different topologies was drawn based on various factors such as power range, system scalability, MPPT effectiveness, overall system efficiency and reliability for residential PV applications.

Section 3 explored the concept of smart PV module and discussed the advantages of the proposed concept. Analysis of the smart PV module in terms of possible power configurations and power architecture was carried out. Auto-connected flyback converter was chosen for the dc-dc converter stage and cascaded H-bridge inverter topology was chosen for the AC stage based on different requirements.

Section 4 explained the control aspect of the smart PV module. First, the Perturb & Observe MPPT algorithm was discussed followed by the control of the dc-dc converters. Subsequently, feed forward control of inverters was proposed for dc link voltage ripple rejection. The latter part of the chapter was dedicated towards the analysis of the proposed feed forward control scheme against the conventional SPWM based on aspects such as dc link capacitor size reduction, improvement in output power quality

and reliability of the system. It was found that with the proposed correction, the dc link capacitor size can be reduced, output power quality can be improved and the system reliability can also be improved by substituting dc link electrolytic capacitors with film capacitors. However, the voltage stress of the power electronic components will be increased.

Section 5 presented a design example for the three cell /pixel configuration of the smart PV module followed by system level simulation results for step change in insolation. The experimental hardware was also discussed and experimental results were finally presented. The experimental results were in agreement with the analysis and the simulation results.

6.2 Future work

An extension of the work would be to explore the following areas for developing the concept into a product:

- Investigation of power electronic components for operation at elevated temperatures.
- Closed loop control of smart PV module for integration to the grid.
- Incorporation of intelligence in the module for enabling communication between different modules and reporting information to the user.
- An analysis of the cost/watt of the system.
- Evaluation of converter sizing and physical mounting on the module.

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